Esercizio 1

Si consideri la porta logica in tecnologia CMOS mostrata in Fig. 3.

a) Determinare la funzione logica svolta dalla porta in forma minima e disegnare la corrispondente porta logica complessa in tecnologia CMOS. Si giustifichino dettagliatamente le scelte effettuate.

b) Determinare l'intervallo di tempo in cui, a seguito di una commutazione alto-basso dell'ingresso, la tensione di uscita ha andamento lineare nel tempo.

c) Calcolare la massima potenza dissipata dal circuito

d) Considerando la capacità di uscita precaricata a *Vdd/2,* stimare il tempo di necessario affinché *Vout* raggiunga il valore a regime quando l'ingresso è il valore logico 1111

e) Determinare i fattori di forma dei transistori pMOS per eguagliare il tempo di transizione HL e LH 100 -> 000 e viceversa

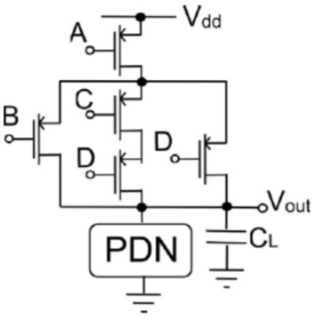


Fig. 3

$V^+ = 2.7\ V$

$\frac{1}{2}\,\mu_n C_{ox} = 100\ \mu A/V^2$

$\frac{1}{2}\,\mu_p C_{ox} = 50\ \mu A/V^2$

$(W/L)_p = 4$

$(W/L)_n = 2$

$|V_{Tp}| = V_{Tn} = 0.7\ V$

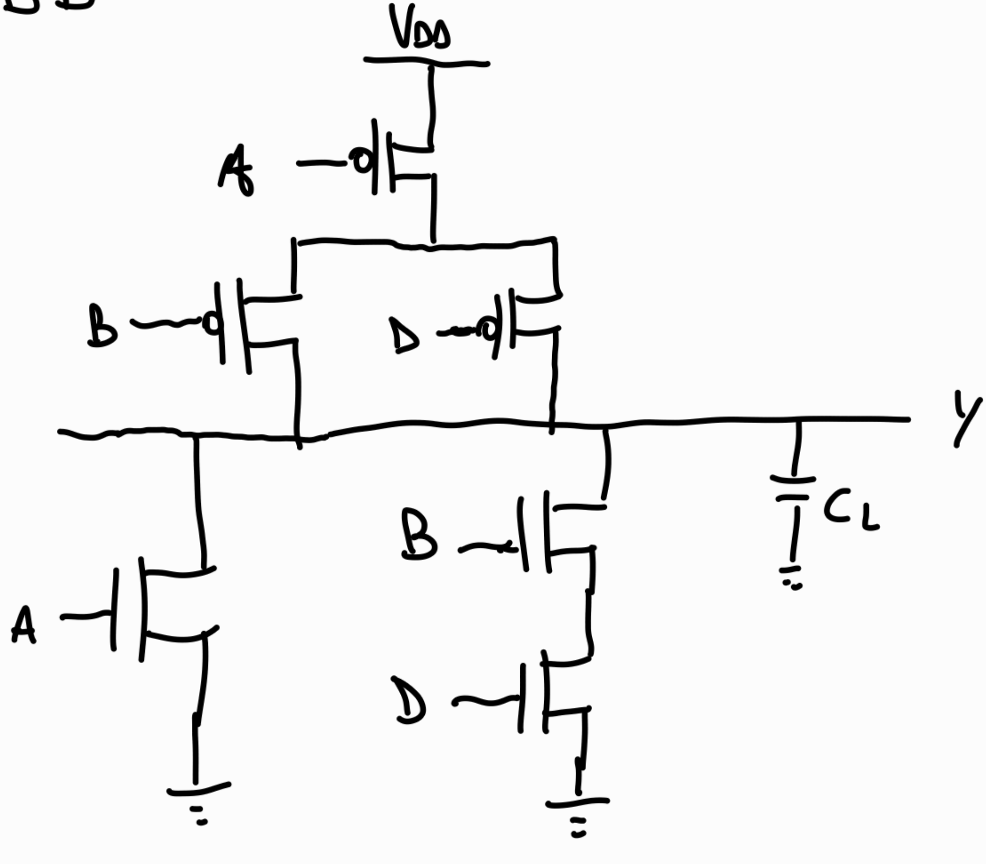
$C_L = 5\ pF$

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}\left[2(V_{GS}-V_T)V_{DS} - V_{DS}^2\right]$$

$$Y = \bar{A}\cdot\left(\bar{B} + \bar{C}\cdot\bar{D} + \bar{D}\right)$$

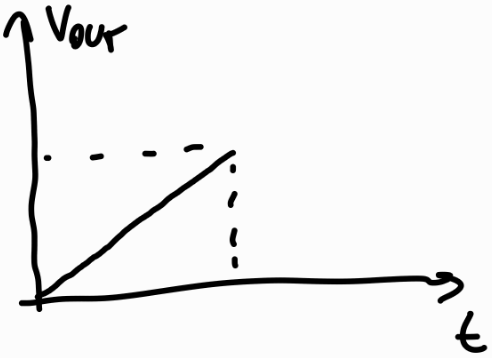
$$= \bar{A}\cdot\left[\bar{B} + \bar{D}\left(\bar{C} + 1\right)\right] = \bar{A}\cdot\left(\bar{B} + \bar{D}\right)$$

$$= \overline{A + BD}$$



b) $\Delta t = ?$ PER CUI $V_{OUT}(t) = \alpha t$

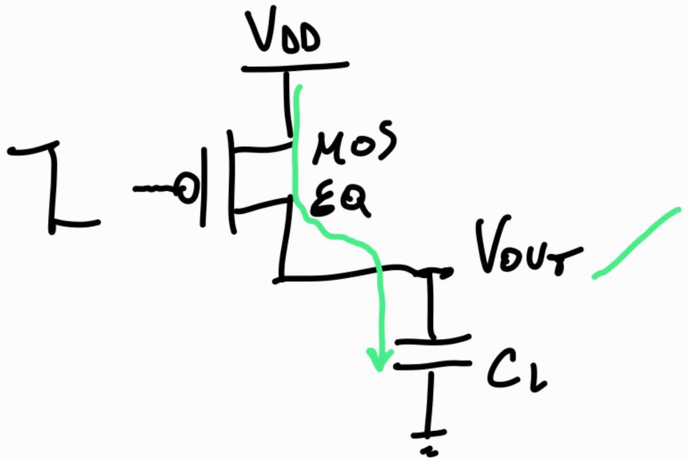
IN ⎿ ⇒ OUT ⌐

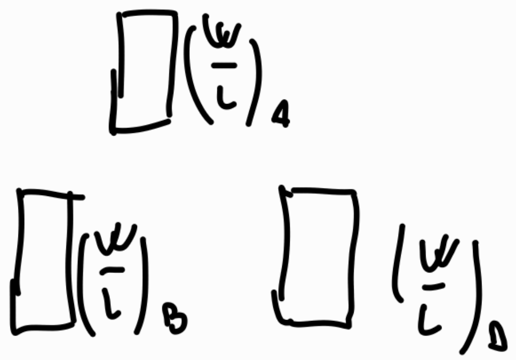


TUTTI GLI INGRESSI CORTO CIRCUITATI

CORRENTE COSTANTE IN USCITA

↳ MOS SONO IN REGIME DI SATURAZIONE





$$\left(\frac{W}{L}\right)_{BD,eq} = \left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_D = 8$$

$$\left(\frac{W}{L}\right)_{P,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_{BD,eq}} + \frac{1}{\left(\frac{W}{L}\right)_{A,eq}}} = \frac{8}{3}$$

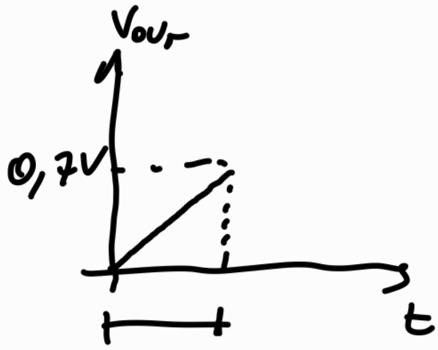
$$|I_P| = \frac{1}{2}\mu_P C_{ox}\left(\frac{W}{L}\right)_{P,eq}\left(V_{GSp} - V_{Tp}\right)^2$$

$$= 133\ \mu A/V^2 \cdot (0 - 2{,}7 + 0{,}7)^2 = 533\ \mu A$$

$V_{GD_p} > V_{Tp} \rightarrow 0 - V_{OUT} > -0,7 \rightarrow V_{OUT} < 0,7V$

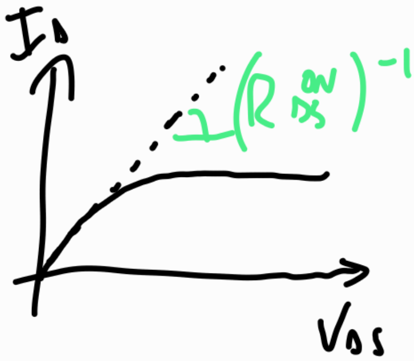
$C = \frac{Q}{V} \rightarrow V_{OUT} = \frac{Q}{C_L} = \frac{I_p \cdot \Delta t}{C_L}$

$\Delta t = \frac{V_{OUT} C_L}{I_p} = 6,57 \ ns$



c) $P_{MAX} = ?$ $\quad P = F_{CK} \cdot V_{DD}^2 \cdot C_L$

$F_{CK}^{MAX} = ? \longrightarrow T_{CK}^{MIN} = t_{pHL} + t_{pLH}$



$t_{pHL} = 0,69 \cdot C_L \cdot Req_n$ ← CASO PIÙ GRAVOSO: C_L SI SCARICA ATTRAVERSO B E D ↳ $\left(\frac{W}{L}\right)_{eq} = 1$

$= 0,69 \cdot C_L \cdot \frac{1}{2K_n(V_{GS_n} - V_T)}$

$= 0,69 \cdot 5pF \frac{1}{2 \cdot 100 \frac{\mu A}{V^2} \cdot 1 \cdot (2,7V - 0,7V)}$

$= 8,63 \ ns$

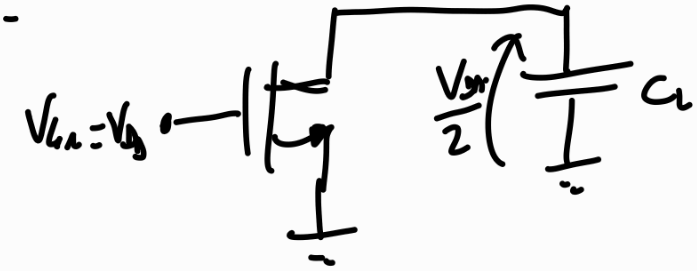
$t_{pLH} = 0,69 \cdot C_L \cdot Req_p$ ← CASO PIÙ GRAVOSO: C_L SI CARICA ATTRAVERSO A E B (OPPURE A E D) ↳ $\left(\frac{W}{L}\right)_{eq} = 2$

$= 0,69 \cdot C_L \cdot \frac{1}{2K_p(V_{GS_p} - V_T)}$

$= 0,69 \cdot 5pF \frac{1}{2 \cdot 50 \frac{\mu A}{V^2} \cdot 2 \cdot (2,7V - 0,7V)} = 8,63 \ ns$

$T_{CK}^{MIN} = 17,26 \ ns \rightarrow F_{CK}^{MAX} = \frac{1}{T_{CK}^{min}} = 58 \ MHz \rightarrow P_{MAX} = 2,1 \ mW$

d) $t = 0^-$



$$\frac{V_{DD}}{2} = 1{,}35\ V$$

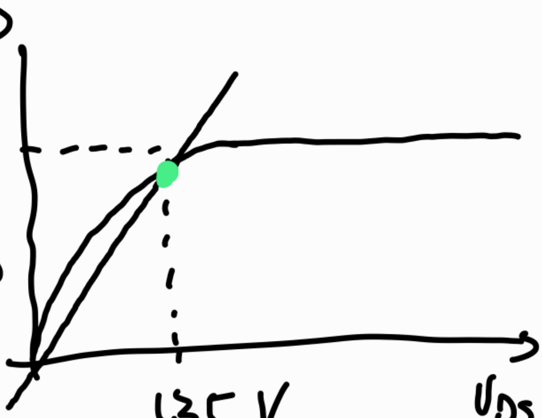
$$V_{GD_M} = \frac{V_{DD}}{2} = 1{,}35\,V > V_{T_M}$$

MOS ZONA OHMICA

APPROX

$$R_{MOS} = \frac{\Delta V}{\Delta I}$$

$$\left(\frac{W}{L}\right)_{M,eq} = \left(\frac{W}{L}\right)_A + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_D}} = 3$$

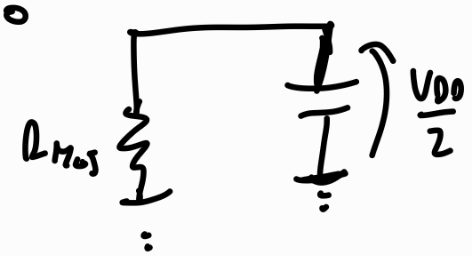


$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M,eq}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]$$

$$= 100\ \mu A/V^2 \cdot 3\left[2\left(2{,}7 - 0{,}7\right)1{,}35 - 1{,}35^2\right] = 1{,}07\ mA$$

$$R_{MOS} = \frac{1{,}35\ V}{1{,}07\ mA} = 1{,}26\ k\Omega$$

$t = 0^+$



$$T_{DIS} \simeq 5 \cdot \tau = 5 \cdot R_{MOS} \cdot C_L \stackrel{!}{=} 31{,}5\ ns$$

e) DIMENSIONARE PMOS

LH $100 \rightarrow 000$

HL $000 \rightarrow 100$

HL) C_L SI SCARICA ATTRAVERSO MOS A

$$\left(\frac{W}{L}\right)_{M,eq} = \left(\frac{W}{L}\right)_n = 2$$

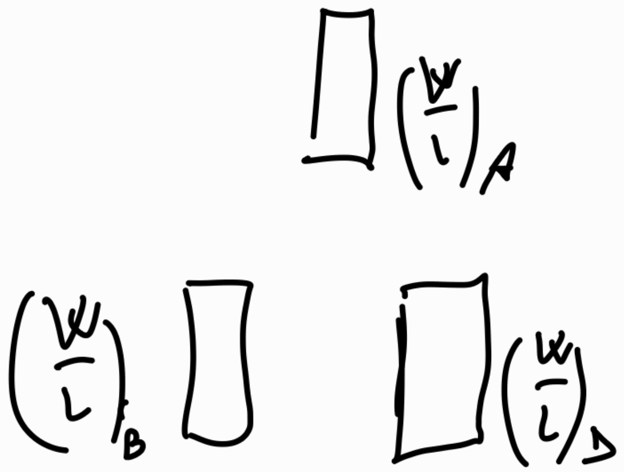
LH) C_L SI CARICA ATTRAVERSO TUTTI I PMOS

$$\left(\frac{W}{L}\right)_{p,eq} = \frac{8}{3}$$ ATTUALE

$$K_{M_{eq}} = |K_{P_{eq}}| \rightarrow 100\mu \left(\frac{W}{L}\right)_{M,eq} = 50\mu \left(\frac{W}{L}\right)_{P,eq}$$

NUOVO

$$\left(\frac{W}{L}\right)_{P,eq} = \frac{100\mu}{50\mu} \left(\frac{W}{L}\right)_{M,eq} = 4$$



$$\left(\frac{W}{L}\right)_B = 4 \qquad \left(\frac{W}{L}\right)_D = 4$$

$$\left(\frac{W}{L}\right)_A = 8$$

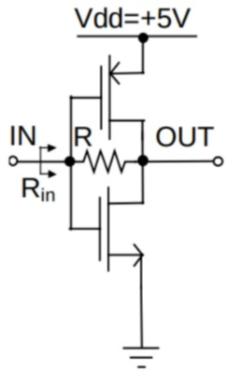
AA 2003/2004 TERZO APPELLO (15/09/2004)

Esercizio 2

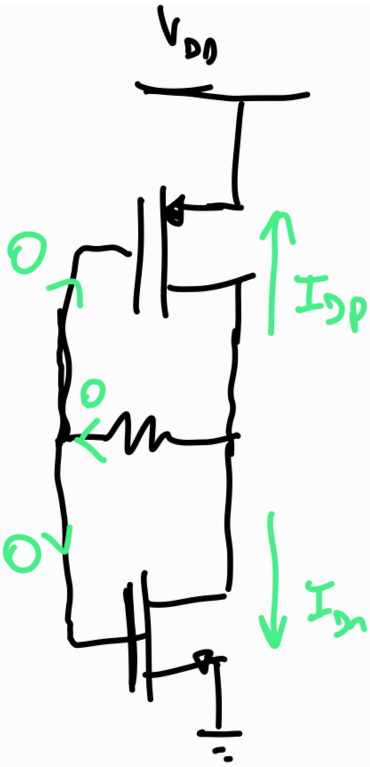
a) **Determinare la tensione in continua al nodo IN e al nodo OUT e la corrente circolante in ognuno dei due MOSFET.**

b) **Determinare il guadagno di piccolo segnale v_{OUT}/v_{IN}.**

c) Determinare il valore della resistenza di ingresso R_{in} indicata in Figura.



$|V_{Tp}|=V_{Tn}=1\text{V}$
$k_n=k_p=1\text{mA/V}^2$
$R=1\text{M}\Omega$



$$I_{Dn} + I_{Dp} = 0$$

$$K_n (V_G - V_{Tn})^2 - |K_p| (V_G - V_{DD} - V_{Tp})^2 = 0$$

$$1\,\frac{mA}{V^2} (V_G - 1)^2 = 1\,\frac{mA}{V^2} (V_G - 5 + 1)^2$$

$$V_G^2 - 2V_G + 1 = V_G^2 - 8V_G + 16$$

$$V_G = 2,5\ V$$

$V_{GDn} < V_{Tn}$
$V_{Gn} = V_{Dn}$ nMOS SATURO
$V_{Gp} = V_{Dp}$ pMOS SATURO

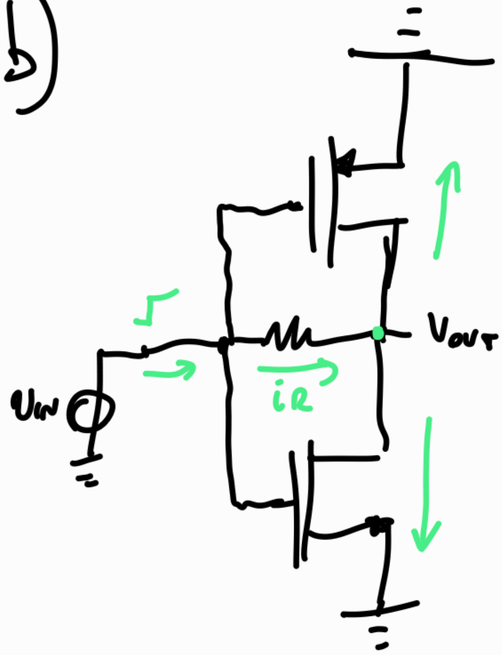
$$I_R = 0 \rightarrow V_{OUT} = 2,5\ V$$

$$I_{Dn} = K_n (V_{GS} - V_{Tn})^2 = 1\,mA/V^2 (2,5 - 1)^2 = 2,25\ mA$$

$$g_{m_n} = 2 K_n (V_{GS} - V_{Tn}) = 3\,mA/V$$

$$g_{m_p} = 3\,mA/V$$

b)



$$i_R = g_{mn} v_{gsn} + g_{mp} v_{gsp}$$

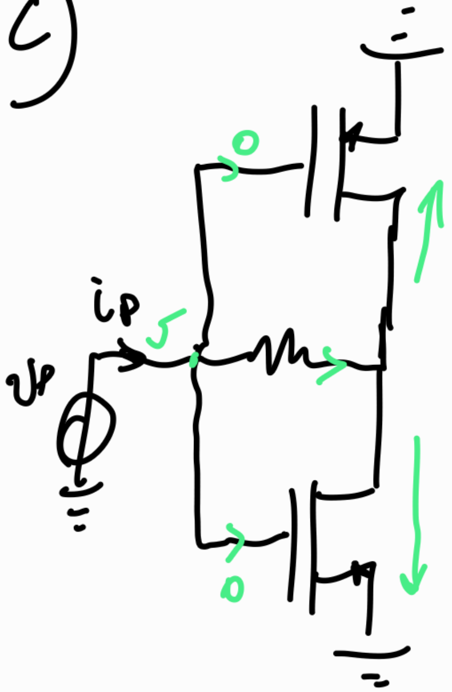
$$v_{OUT} = v_{IN} - i_R \cdot R$$

$$= v_{IN} - R\left(g_{mn} v_{IN} + g_{mp} v_{IN}\right)$$

$$= v_{IN}\left[1 - R\left(g_{mn} + g_{mp}\right)\right]$$

$$\frac{v_{OUT}}{v_{IN}} = 1 - R\left(g_{mn} + g_{mp}\right) = -5999$$

c)



$$\frac{v_p}{i_p} = R_{IN}$$

$$i_p = v_p\left(g_{mn} + g_{mp}\right)$$

$$R_{IN} = \frac{1}{g_{mn} + g_{mp}} = 166\ \Omega$$