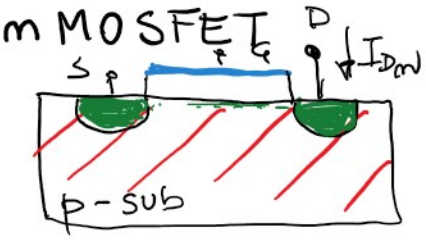
Transistore MOSFET

lunedì 23 marzo 2020 10:33



- $V_{T_n} > 0$, canale di elettroni
- substrato di tipo p
- zona ohmica

  $V_{GS_n} > V_{T_n}$ canale lato source

  $V_{GD_n} > V_{T_n}$ canale lato drain

  $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[2(V_{GS_n} - V_{T_n}) V_{DS_n} - V_{DS_n}^2 \right]$

  k_n FATTORE DI TRANSCONDUTTANZA

  $[k_n] = \frac{I}{V^2}$ $\frac{mA}{V^2}$

  $k_n > 0$

- zona di saturazione

  $V_{GS_n} > V_{T_n}$ canale lato source

  $V_{GD_n} < V_{T_n}$ no canale lato drain (pinch-off).

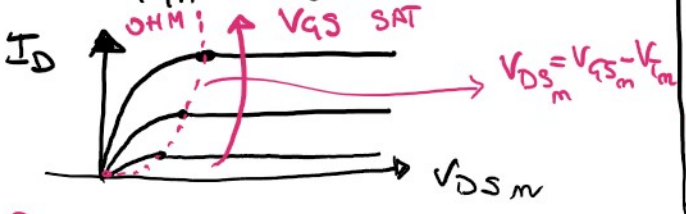
  $I_D = k_n (V_{GS_n} - V_{T_n})^2$

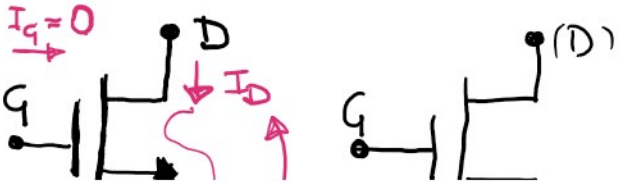
- MOS spento

  $V_{GS_n} < V_{T_n}$

  $V_{GD_n} < V_{T_n}$ non c'è canale

$V_{GS} > V_{T_n}$ — MOS on





- substrato di tipo n
- $V_{T_p} < 0$, canale di lacune
- MOS off, no canale

  $V_{GS_p} > V_{T_p}$

  $V_{GD_p} > V_{T_p}$

- MOS acceso

  $V_{GS_p} < V_{T_p}$ canale lato source

* $V_{GD} < V_{T_p}$ canale lato drain

⇓ ZONA OHMICA

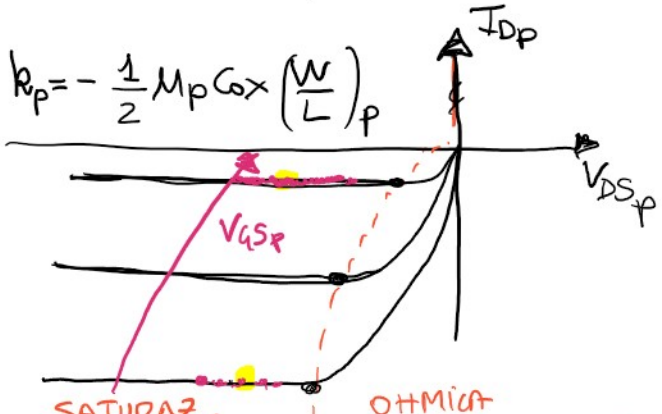
$I_{D_p} = k_p \left[2(V_{GS_p} - V_{T_p}) V_{DS_p} - V_{DS_p}^2 \right]$

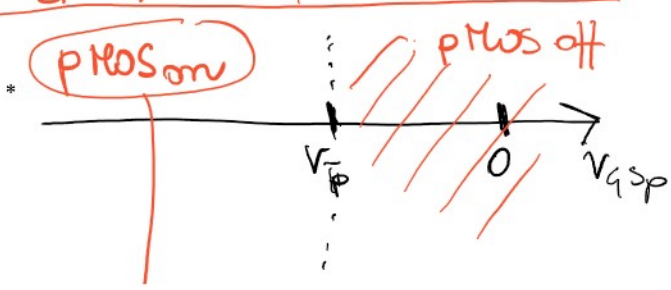
* $V_{GD} > V_{T_p}$ no canale lato drain (pinch-off lato drain)

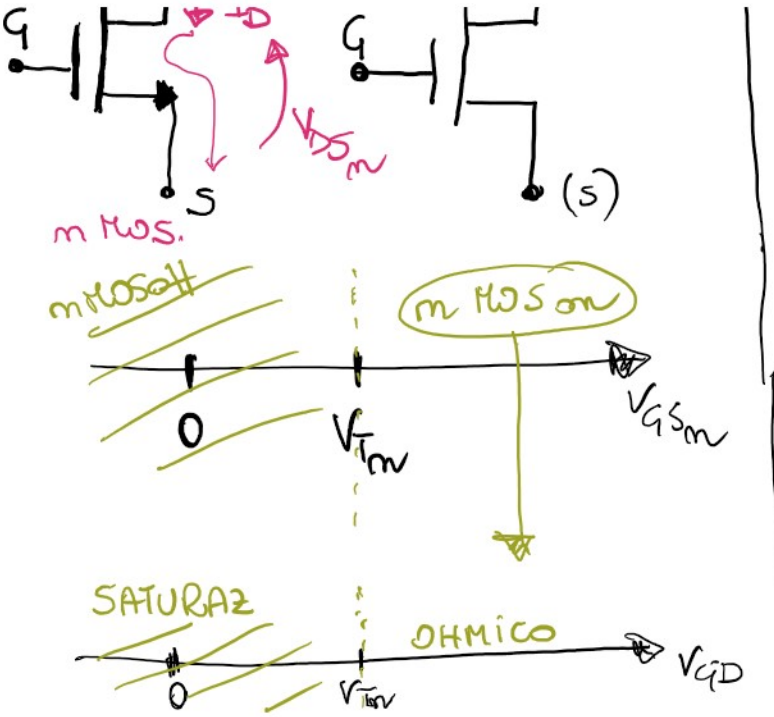
⇓ ZONA DI SATURAZIONE

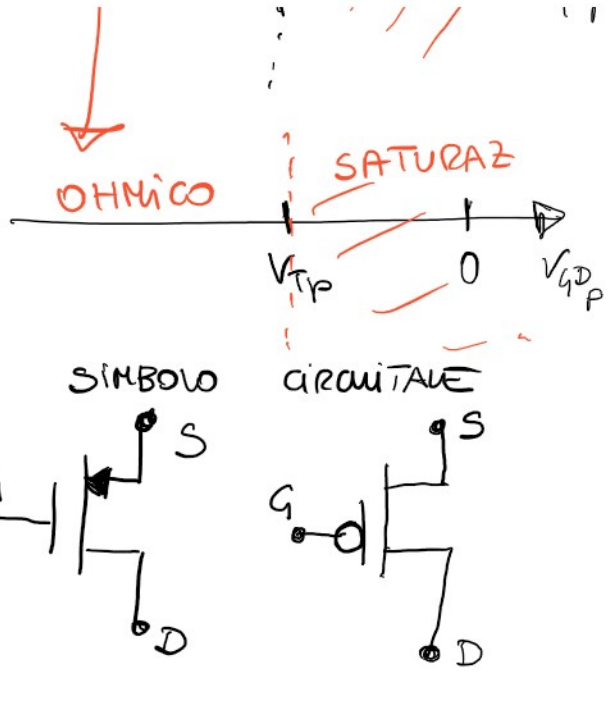
$I_{D_p} = k_p (V_{GS_p} - V_{T_p})^2$

$k_p = -\frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p$

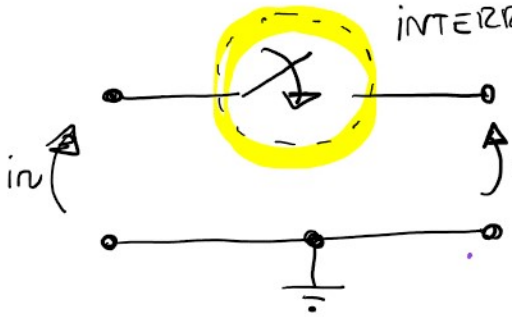








TRANSISTORE MOS come INTERRUTTORE



- INTERRUTTORE APERTO (circ. aperto) — OUT e IN scollegati (MOS spento)
- INTERRUTTORE CHIUSO (corto circuito) — OUT e IN cortocircuitati (MOS acceso in zona ohmica)

MOS acceso in zona ohmica – Resistenza di canale

$$R_{DS_{on}} \triangleq \left.\frac{\partial V_{DS}}{\partial I_{D_{ohm}}}\right|_{V_{DS}=0} = \left[\left.\frac{1}{\frac{\partial I_{D,ohm}}{\partial V_{DS}}}\right|_{V_{DS}=0}\right] = \frac{1}{2k_n(V_{GS_n}-V_{T_n})} =$$

(mMOS)

$$I_{D_{ohm}} = k_n\left[2(V_{GS_m}-V_{T_m})V_{DS_m} - V_{DS_m}^2\right]$$

$\begin{cases} V_{GS_m} > V_{T_m} \\ V_{GD_m} > V_{T_m} \end{cases}$ ZONA OHMICA

$$\frac{\partial I_{D_{ohm}}}{\partial V_{DS}} = 2k_n(V_{GS}-V_{T_m}) - 2k_n V_{DS_m} \quad (V_{DS_m}=0)$$

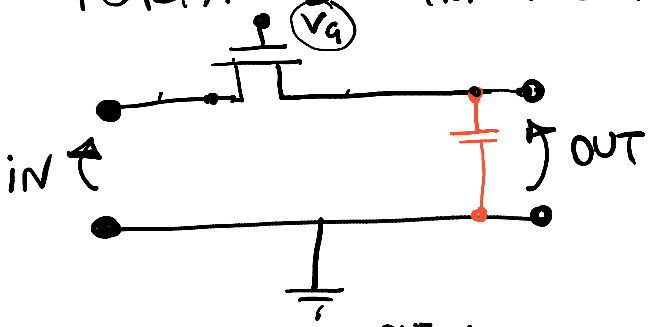
$$R_{DS_{on}} = \frac{1}{2\left[\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS_m}-V_{T_m})\right]}$$

$$R_{DS_{on}} = \frac{1}{2\left[\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS_n} - V_{T_n}\right)\right]}$$

FATTORE DI FORMA $\frac{W}{L}$

TENSIONE DI OVERDRIVE $V_{GS_n} - V_{T_n}$

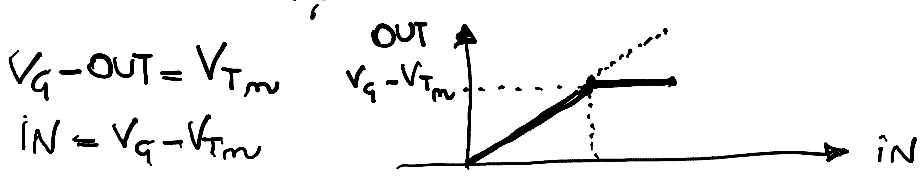
PORTA DI TRASMISSIONE nMOS

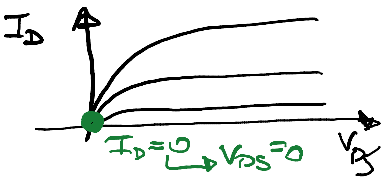


* $\begin{cases} V_{GS} < V_{Tn} \\ V_{GD} < V_{Tn} \end{cases} \Rightarrow$ nMOS off

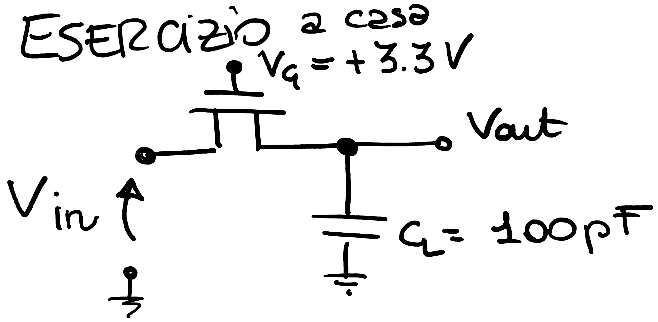
IN e OUT scollegati

* $V_{GS} > V_{Tn}$ nMOS on





ESERCIZIO a casa



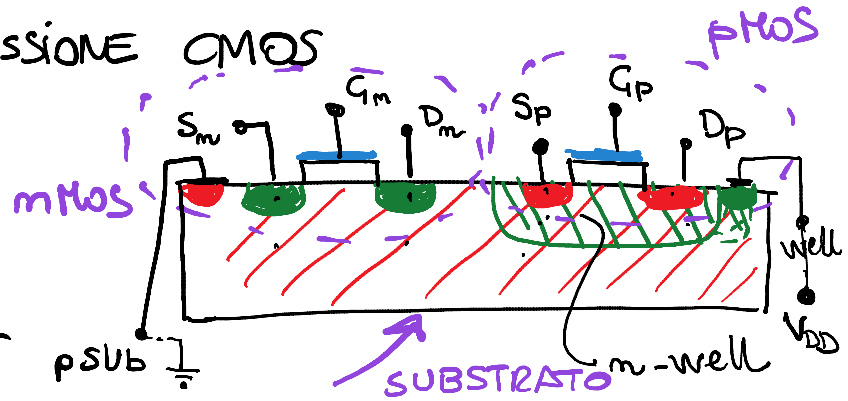
$V_{Tn} = 0.8\,V$

(a) Vout se $V_{in} = 0\,V$? (esauriti transitori)

(b) Vout se $V_{in} = 3.3\,V$? (esauriti transitori)

PORTA DI TRASMISSIONE CMOS

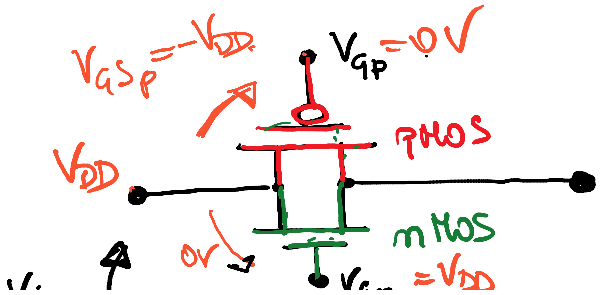
Complementary
Metal
Oxide
Semiconductor



* $V_{G_n} = 0V$, $V_{G_p} = 5V = V_{DD}$

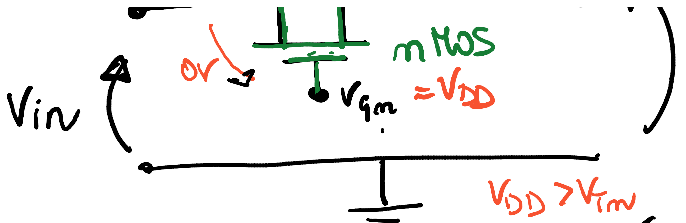
$V_{in} = 0V$ ⇓ nMOS pMOS interdetti

in e out sono scollegati



* $V_{G_n} = V_{DD}$ $V_{G_p} = 0V$

$V_{in} = 0V$



$V_{DD} > V_{in}$

$V_{in} \in [0, V_{DD}]$ $V_{DD} = 5V$

V_{G_P} deve essere duale rispetto al nMOS

ad es. $V_{G_n} = 0V$

$\Downarrow$

$V_{G_P} = V_{DD} (= 5V)$

* $V_{G_n} = V_{DD}$ $V_{G_P} = 0V$

$V_{in} = 0V$

nMOS on

$I_D = 0 \Rightarrow V_{DS} = 0$

$\Downarrow$ $V_{out} = 0$

pMOS interdetto

* $V_{G_n} = V_{DD}$, $V_{G_P} = 0V$

$V_{in} = V_{DD}$

pMOS acceso

$\Downarrow$ $\boxed{V_{out} = V_{DD}}$

$\boxed{V_{out} = V_{in}}$

☺ $V_{out} = V_{in}$ senza necessità di V_G maggiori dell'intervallo di tensioni di V_{in}

☺ $R_{ds_{on_{TOT}}} = R_{ds_{on_n}} // R_{ds_{on_P}}$ più piccolo di quello di un solo Transistore

☹ 2 Transistori complementari con tensioni di comando duali