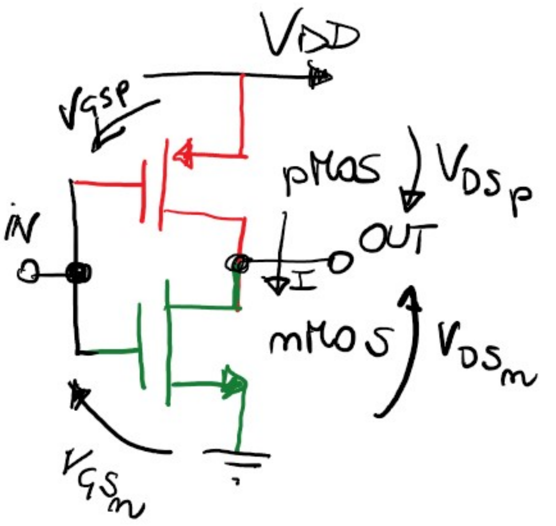
Inverter CMOS

mercoledì 25 marzo 2020 10:34



Hp $V_{DD} > V_{Tn}$

$V_{GS_n} = IN - 0 = IN$.

$V_{DS_n} = OUT - 0 = OUT$

$V_{GS_p} = IN - V_{DD}$

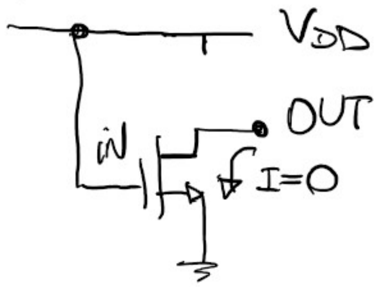
$V_{DS_p} = OUT - V_{DD}$

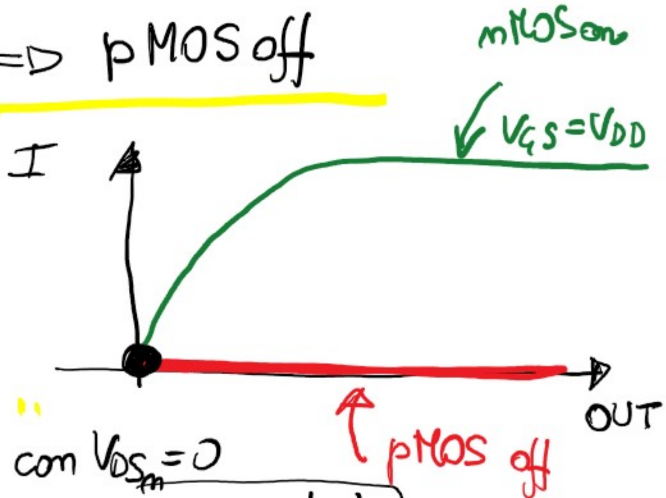
$V_{Tn} = |V_{Tp}| = V_T$.

- $IN = '1' \Rightarrow IN = V_{DD}$

$V_{GS_n} = V_{DD} > V_{T_n} \Rightarrow$ nMOS on

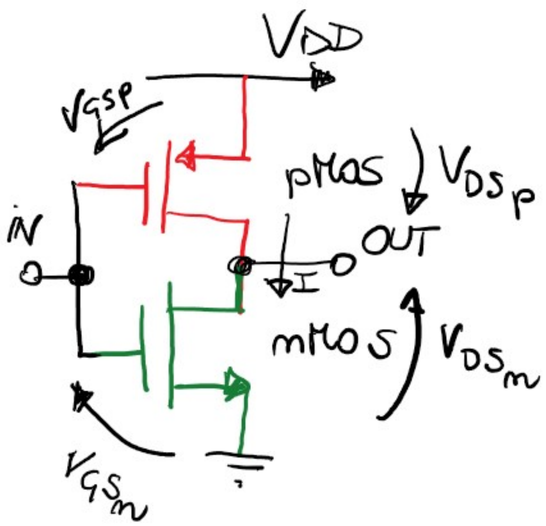
$V_{GS_p} = V_{DD} - V_{DD} = 0 \Rightarrow$ pMOS off





↳ nMOS ohmico con $V_{DS_n} = 0$

↳ $OUT = 0V \Rightarrow OUT = '0'$ ok



$V_{GS_p} = IN - V_{DD}$

$V_{DS_p} = OUT - V_{DD}$

$I = -I_{D_p}$

$OUT = V_{DS_p} + V_{DD}$

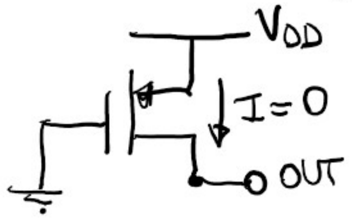
V_{GS_n}

$OUT = V_{DS_p} + V_{DD}$

- **IN = '0'** $\Rightarrow V_{GS_n} = 0 < V_{T_n} \Rightarrow$ nMOS off

$V_{GS_p} = 0 - V_{DD} = -V_{DD} < V_{T_p}$

↳ pMOS on



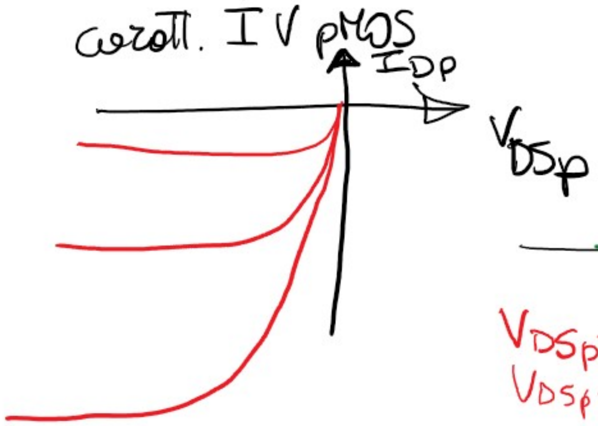
$I = 0$

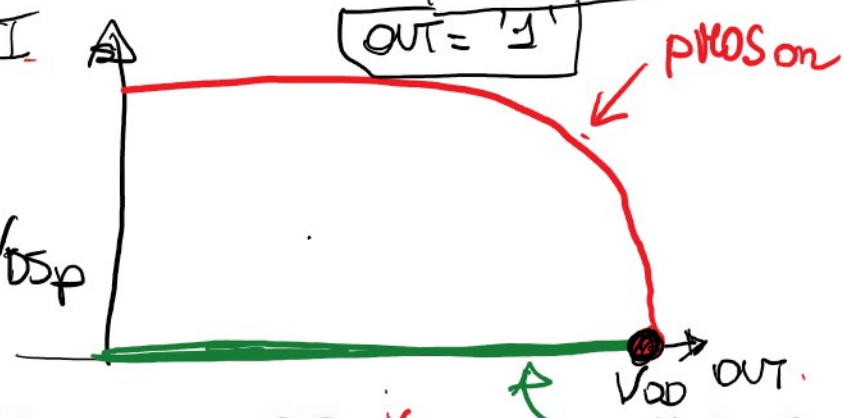
↳ $V_{DS_p} = 0$

⇓ $OUT = V_{DD}$

OUT = '1'

caratt. IV pMOS





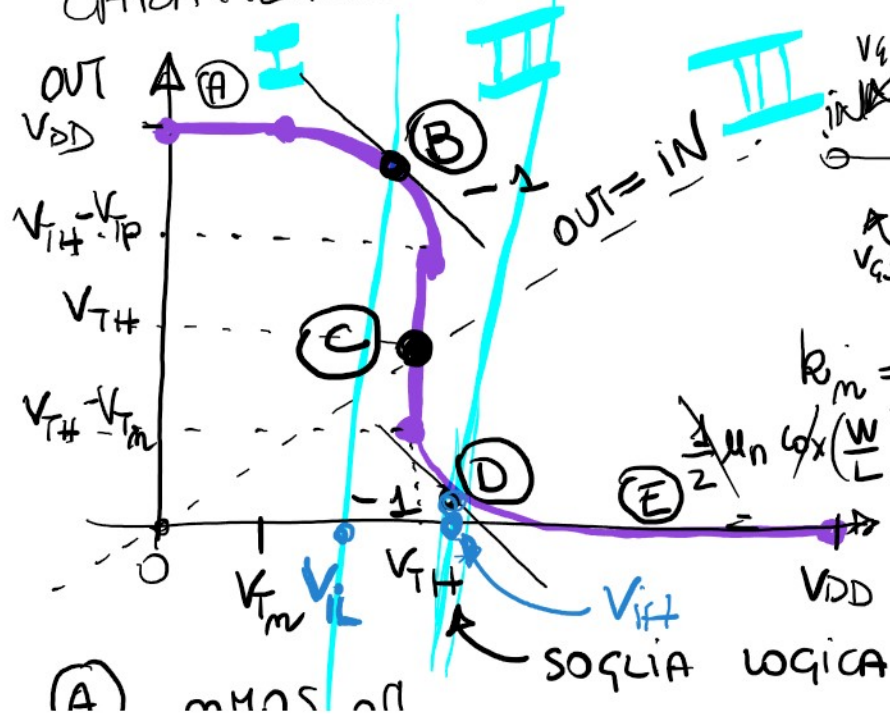
$V_{DS_p} = 0 \Rightarrow OUT = V_{DD}$

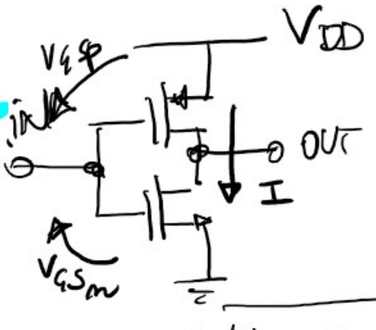
$V_{DS_p} = -V_{DD} \Rightarrow OUT = 0$

$I_{statica} = 0$ sia per IN = '0' che per IN = '1'

↳ $P_{STAT} = 0$. DISS. POTENZA STATICA NULLA!

CARATTERISTICA DI TRASFERIMENTO STATICA





$k_n = |k_p|$ INVERTER SIMMETRICO

$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p$

$\mu_n\left(\frac{W}{L}\right)_n = \mu_p\left(\frac{W}{L}\right)_p$

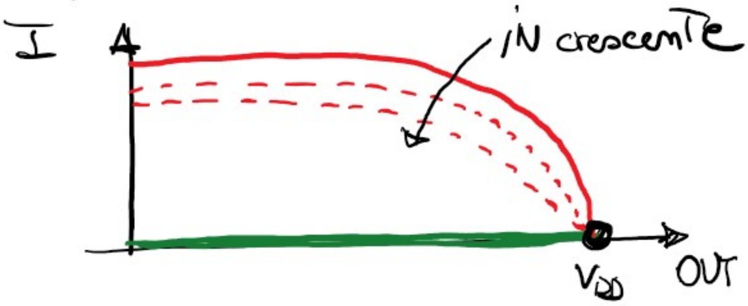
(A) nMOS off

SOGLIA LOGICA

$\mu_n \left(\frac{W}{L}\right)_n = \mu_p \left(\frac{W}{L}\right)_p$

(A) nMOS off

pMOS on in zona ohmica



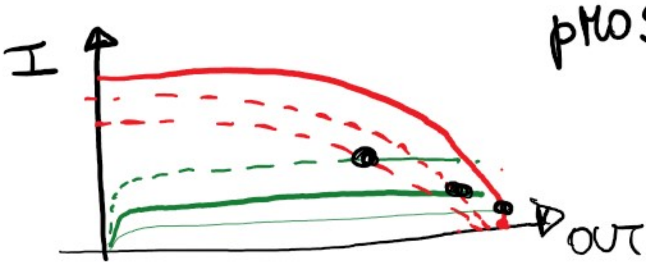
$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p} \left(\frac{W}{L}\right)_n = 2.5 \left(\frac{W}{L}\right)_n$$

$\mu_n \simeq 800\ cm^2/Vs$

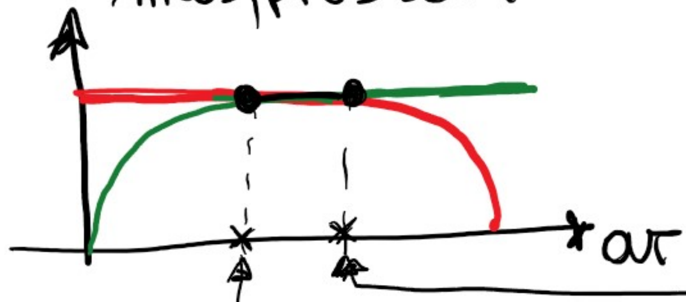
$\mu_p \simeq 300\ cm^2/Vs$

(B) nMOS on in zona di saturazione

pMOS on in zona ohmica



(C) nMOS, pMOS saturi



pMOS

$V_{DS_p} = V_{GS_p} - V_{T_p}$

$OUT - V_{DD} = IN - V_{DD} - V_{T_p}$

$OUT = V_{TH} - V_{T_p}$

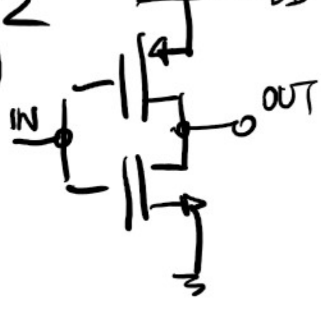
$V_{DS_n} = V_{GS_n} - V_{T_n} = V_{TH} - V_{T_n}$

CALCOLO DELLA SOGLIA LOGICA

$$I_{D_{n\,SAT}} = |I_{D_{p\,sat}}|$$

$$k_n (V_{GS_n} - V_{T_n})^2 = |k_p| (V_{GS_p} - V_{T_p})^2$$

inverter simmetrico $k_n = |k_p|$



$$(IN - V_{T_n})^2 = \left[(IN - V_{DD}) - V_{T_p}\right]^2$$

$$(IN - V_{Tm}) = \left[(IN - V_{DD}) - V_{Tp} \right]$$

$$V_{Tm} = |V_{Tp}| = V_T > 0$$

$$(IN - V_T)^2 = \left[(IN - V_{DD}) + V_T \right]^2$$

estraggo le radici quadrate

$$IN - V_T = - \left[(IN - V_{DD}) + V_T \right]$$

$$IN - \cancel{V_T} = - IN + V_{DD} - \cancel{V_T}$$

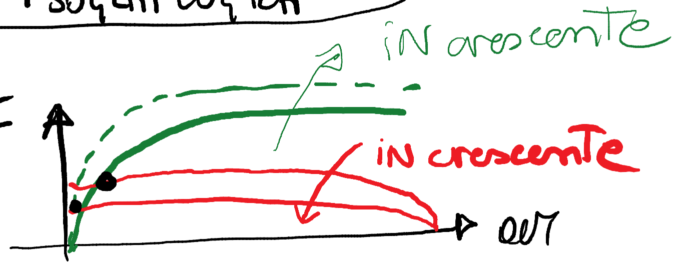
$$2 IN = V_{DD}$$

$$\Downarrow$$

$$IN \Big|_{\text{soglia logica}} \triangleq V_{TH} = \frac{V_{DD}}{2}$$

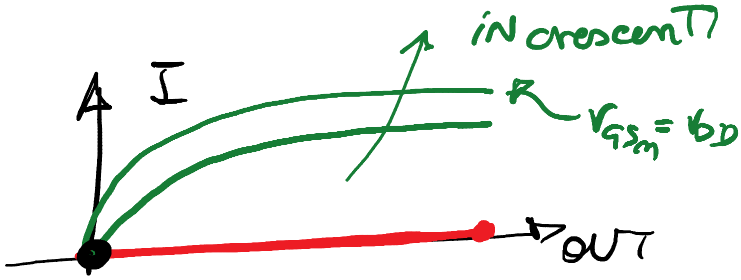
. SOGLIA LOGICA DI COMMUTAZIONE

(D)



nMOS ohmico
pMOS saturo

(E) pMOS off
nMOS ohmico



V_{iL} = max iN interpretato come livello logico basso

V_{iH} = MIN iN interpretato come livello logico alto.

EFFETTO DELLA TENS. DI ALIMENTAZ.

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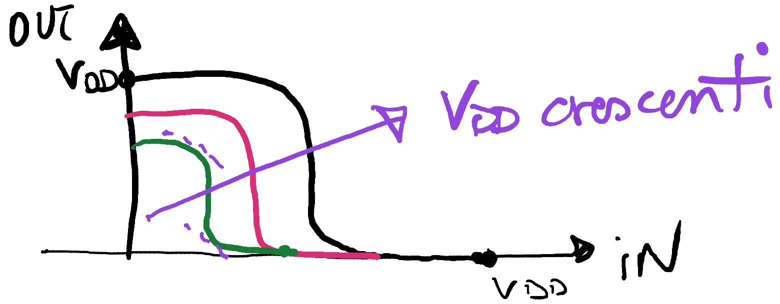
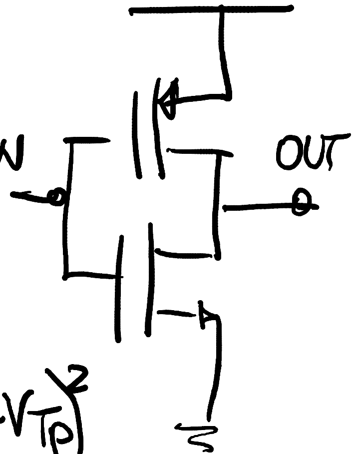
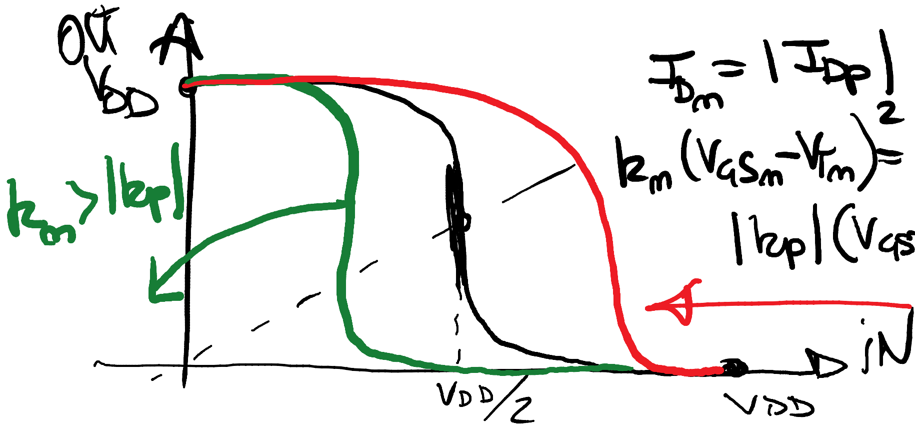


INVERTER NON SIMMETRICO





$I_{Dn} = |I_{Dp}|$

$k_n (V_{GSn} - V_{Tn})^2 = |k_p| (V_{GSp} - V_{Tp})^2$

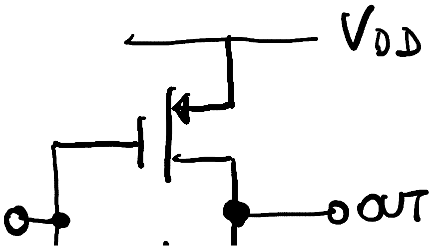
INVERTER AREA MINIMA

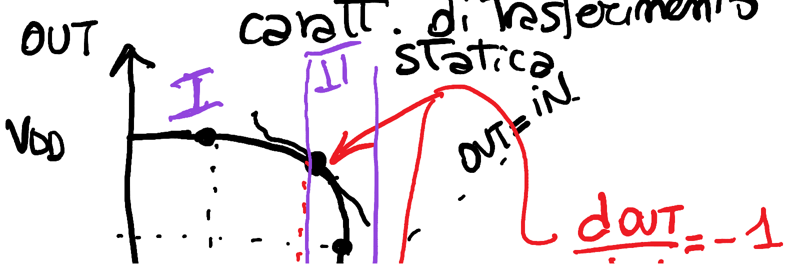
$$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n$$

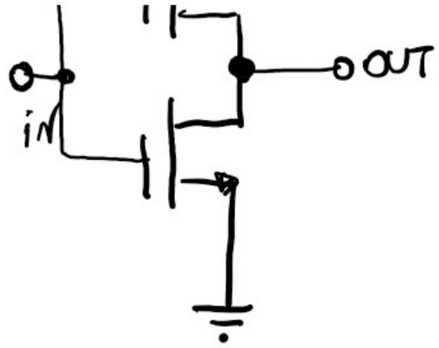
⇓

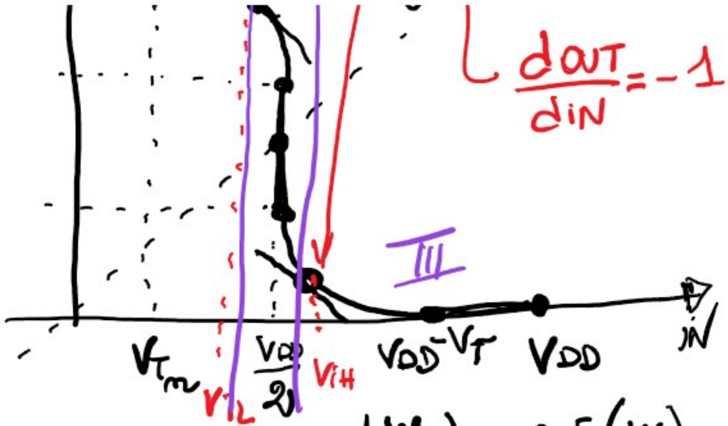
$|k_p| \neq k_n \qquad |k_p| \doteq \frac{k_n}{2.5}$ ← rapporto di mobilità

INVERTER CMOS - MARGINI DI RUMORE (NOISE MARGINS)









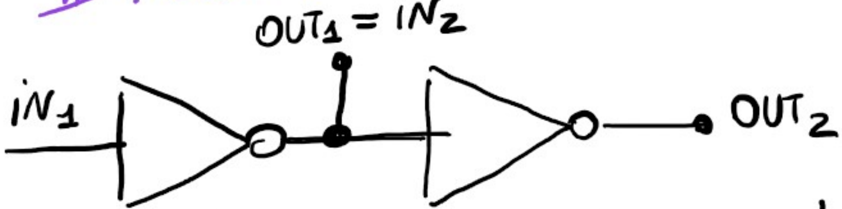
$V_{T_n} = |V_{T_p}| = V_T$

$k_n = |k_p|$ INVERTER SIMMETRICO $\left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$

V_{iL} tale che $\forall$ $iN < V_{iL} \Rightarrow OUT =$ '1'

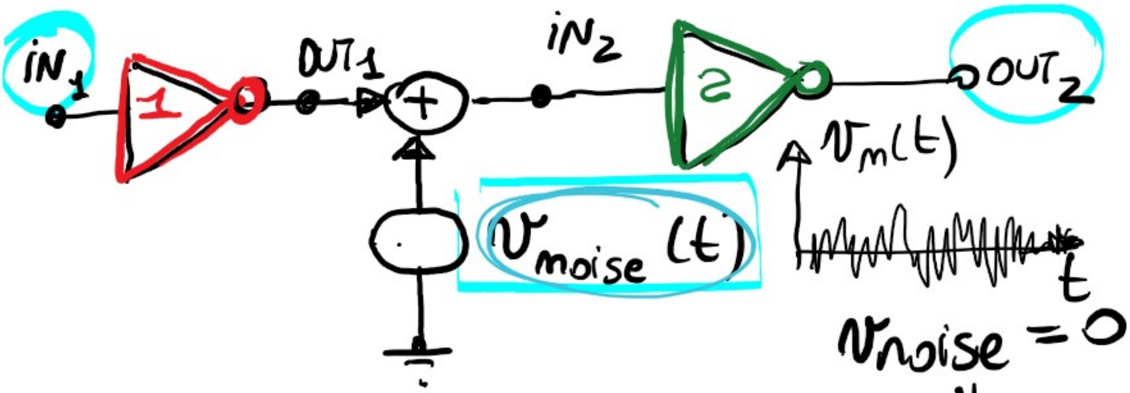
V_{iH} tale che $\forall$ $iN > V_{iH} \Rightarrow OUT =$ '0'

II : ZONA DI TRANSIZIONE



$iN_1 =$ '1' $\Rightarrow$ $OUT_1 =$ '0' $\Rightarrow$ $iN_2 =$ '0' $\Rightarrow$ $OUT_2 =$ '1'

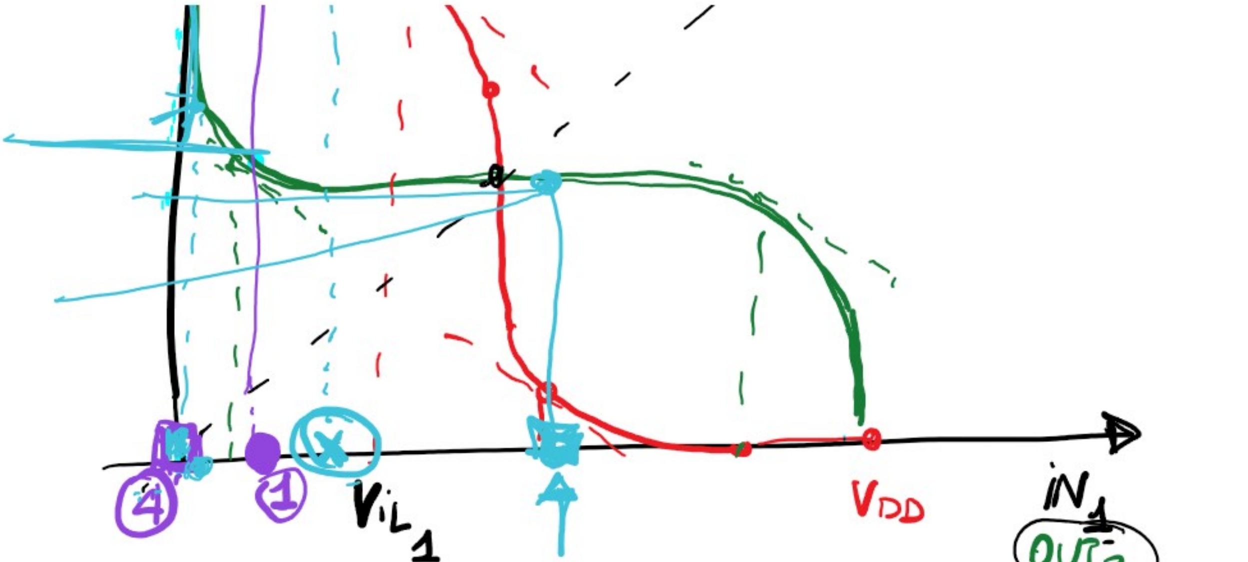
$\left[OUT_2 = \overline{iN_2} = \overline{OUT_1} = \overline{\overline{iN_1}} = iN_1 \right]$



$v_{noise} = 0$

$\Downarrow$

$\boxed{iN_2 = OUT_1 + v_{noise}(t)}$ $\rightsquigarrow$ $OUT_2 = iN_1$



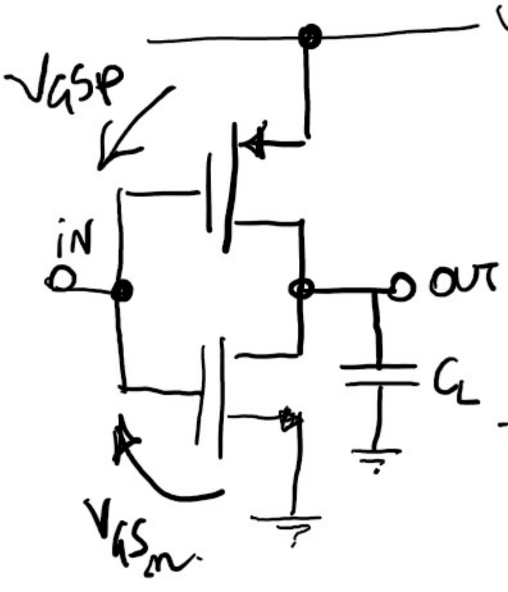
$NM_L \triangleq V_{iL} - 0 = V_{iL}$ noise margin low

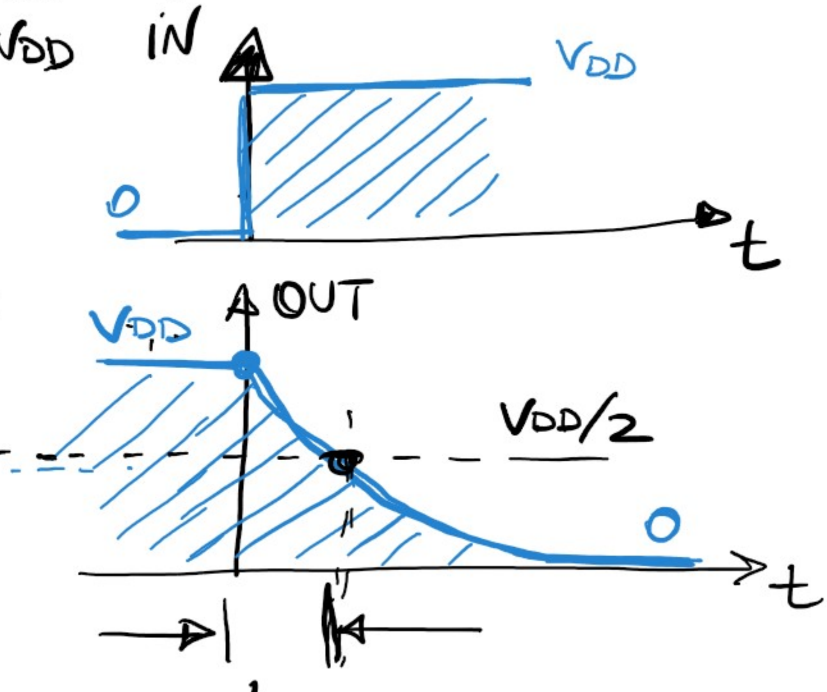
$NM_H \triangleq V_{DD} - V_{iH}$ noise margin high

inverter simmetrico

$NM_L = NM_H$

COMPORTAMENTO DINAMICO DELL' INVERTER CMOS



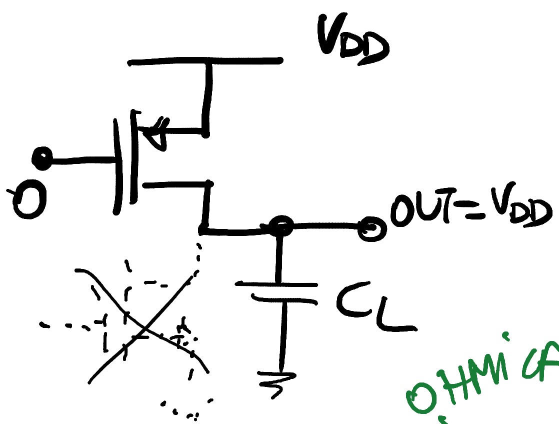


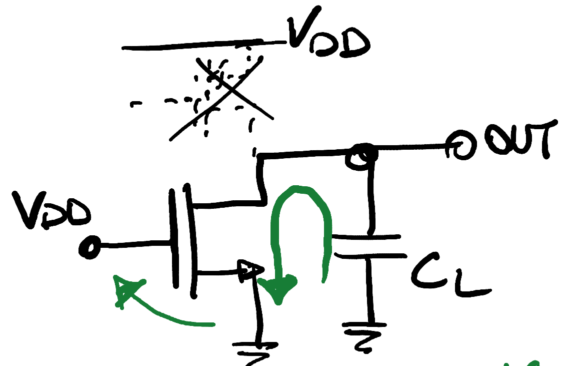
t_{PHL} : TEMPO DI PROPAGAZIONE ALTO-BASSO: tempo necessario perché l'uscita raggiunga il 50% del suo valore ($V_{DD}/2$).

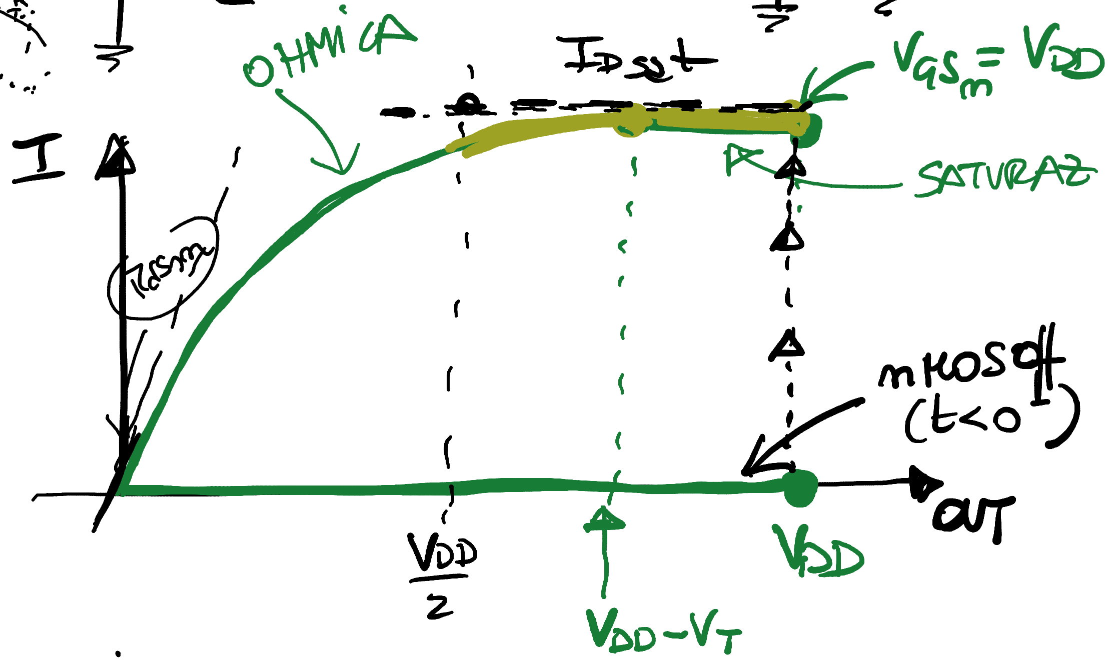
ga il 50% del suo valore ($V_{DD}/2$).

$t_{p_{LH}}$: TEMPO DI PROPAGAZIONE BASSO-ALTO
tempo necessario perché $V_{out} = \frac{V_{DD}}{2}$.

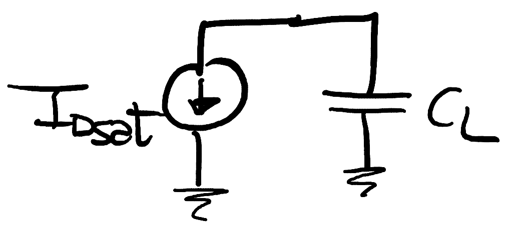
$t \leq 0^-$ | $t \geq 0^+$







APPROSSIMAZIONE SATURA



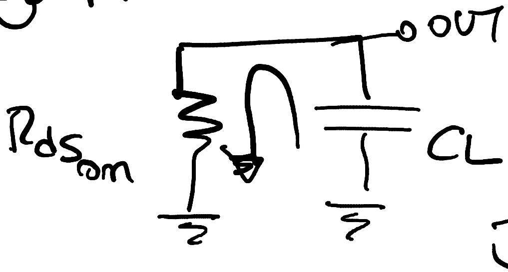
$$I_{Dsat} = k_m (V_{GS} - V_{Tm})^2 = $$
$$= k_m (V_{DD} - V_{Tm})^2$$

$$t_{p_{HL}} = \frac{Q_{50\%}}{I_{Dsat}} = \frac{C_L (V_{DD} - V_{DD}/2)}{k_m (V_{DD} - V_{Tm})^2} =$$

$$= \frac{C_L \, V_{DD}/2}{k (V_{..} - V_{T..})^2}$$

$$= \frac{C_L \; V_{DD}/2}{k_n (V_{DD}-V_{Tn})^2}$$

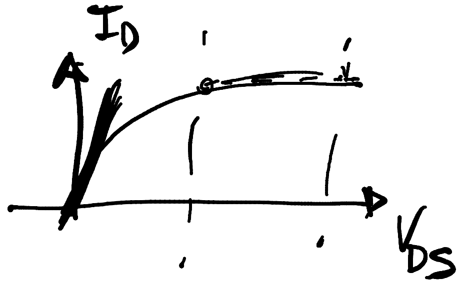
① APPROSSIMAZIONE OHMICA

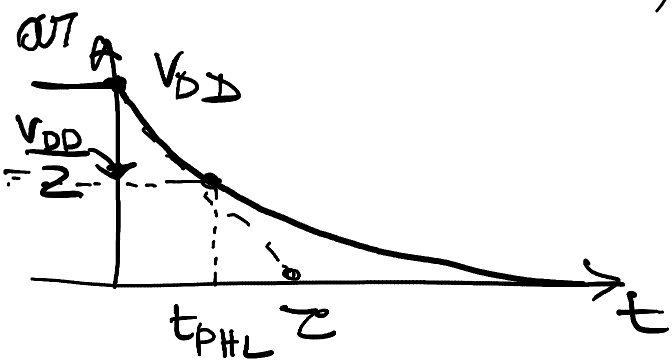


(2) $\tau = R_{ds_{on}} C_L$

(1) $R_{ds_{on}} \triangleq \left.\frac{\partial V_{DS}}{\partial I_{D\,ohm}}\right|_{V_{DS}=0} = \frac{1}{2k_n(V_{DD}-V_{Tn})}$

$$OUT = V_{DD} \exp\left(-t/\tau\right)$$





$$\frac{V_{DD}}{2} = V_{DD} \exp\left(-\frac{t_{pHL}}{\tau}\right)$$

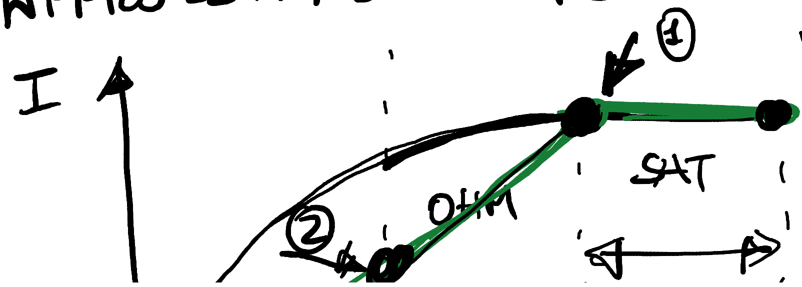
$$\frac{1}{2} = \exp\left(-\frac{t_{pHL}}{\tau}\right)$$

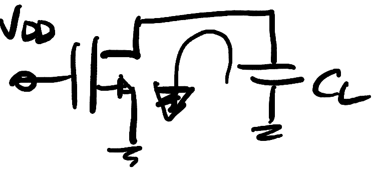
$$\ln\frac{1}{2} = \ln\left[\exp\left(-\frac{t_{pHL}}{\tau}\right)\right]$$

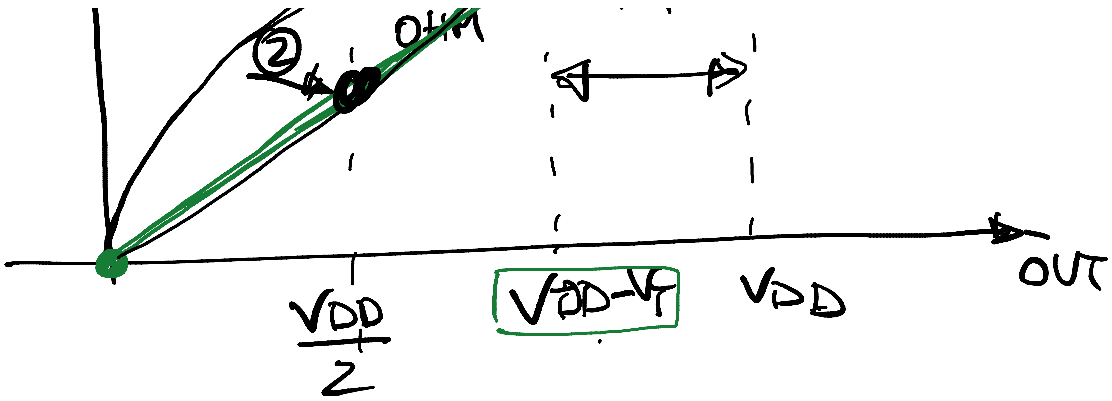
$$\ln 1/2 = -\frac{t_{pHL}}{\tau}$$

$$\boxed{t_{pHL} = \tau \ln 2 = 0.69\,\tau} \quad (3)$$

② APPROSSIMAZIONE PER ECCESSO







$$t_{pHL} = t_{pHL_{sat}} + t_{pHL_{OHM}}$$

- $$t_{pHL_{sat}} = \frac{Q(V_{DD} - (V_{DD}-V_T))}{I_{Dsat}} = \frac{C_L(V_{DD} - V_{DD} + V_T)}{I_{Dsat}} =$$

$$I_{Dsat} = k_n (V_{GS} - V_{Tn})^2 = k_n (V_{DD} - V_{Tn})^2$$

$$= \frac{C_L V_T}{k_n (V_{DD} - V_{Tn})^2}$$

- $t_{pHL_{ohm}}$

$$R_{eq} = \frac{[V_{DD} - V_T - 0]}{I_{Dsat}} = \frac{V_{DD} - V_T}{k_n (V_{DD} - V_{Tn})^2}$$

$$\tau = C_L R_{eq}$$

$$OUT = (V_{DD} - V_T) \exp(-t/\tau)$$

$$\frac{V_{DD}}{2} = (V_{DD} - V_T) \exp(-t/\tau)$$

$$\frac{\frac{V_{DD}}{2}}{V_{DD} - V_T} = \exp(-t/\tau)$$

$$\ln \frac{V_{DD}/2}{V_{DD}-V_T} = - \frac{t_{pHL\,ohm}}{\tau}$$

$$\boxed{t_{pHL_{ohm}} = \tau \ln \frac{V_{DD}-V_T}{V_{DD}/2}}$$

$$\Downarrow \; t_{pHL} = t_{pHL_{ohm}} + t_{pHL\,saturaz.}$$

$$\tau_p \triangleq \frac{t_{pHL} + t_{pLH}}{2}$$

inverter simmetrico

$$\boxed{t_{pHL} = t_{pLH}}$$

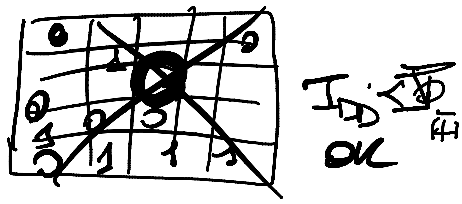
↑ RITARDO DI PROPAGAZIONE

DISSIPAZIONE DI POTENZA INVERTER CMOS

★ POTENZA STATICA

$$\underline{P_{STATICA} = 0}$$

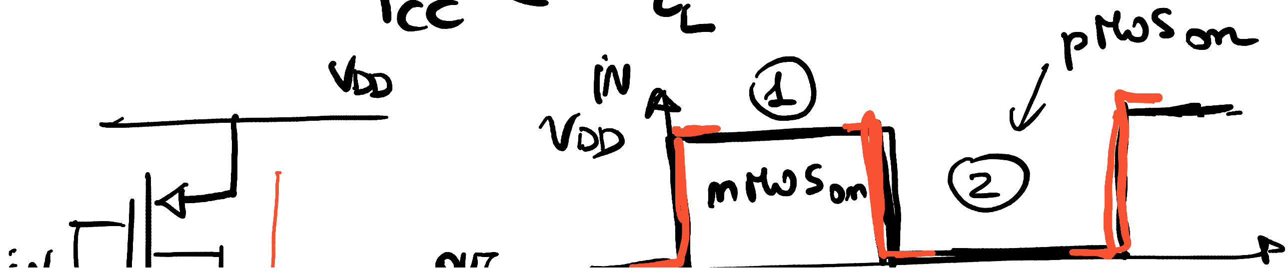
TEST I_{DDQ}

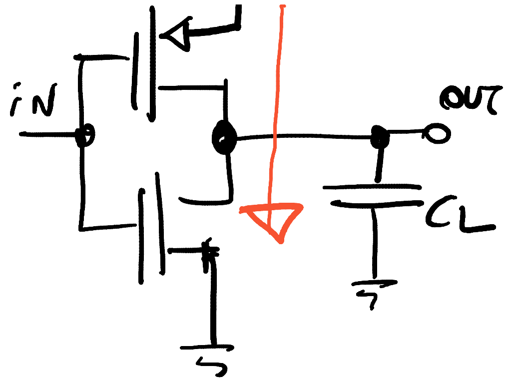


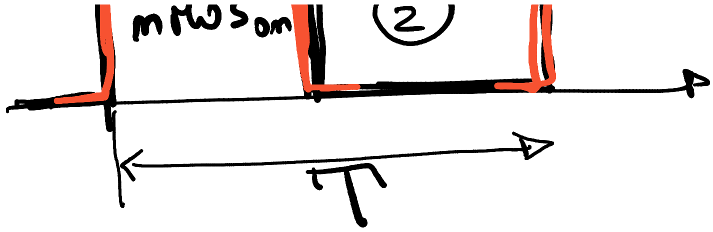
★ POTENZA DINAMICA

- Potenza spesa per la carica e scarica della capacità (P_{CL})
- Potenza di cross-conduzione (P_{CC})

$$P_{CC} \ll P_{CL}$$







$$f = 1/T$$

① C_L è carica a V_{DD}

$E = \frac{1}{2} C_L V_{DD}^2$

Durante T_e la scarica E è dissipata dall'nMOS

② $E = \int i(t)\, v(t)\, dt =$

$= V_{DD} \int i(t)\, dt = V_{DD}\, C_L V_{DD} =$

$= C_L\, V_{DD}^2$ → $\frac{1}{2} C_L V_{DD}^2$ in C_L

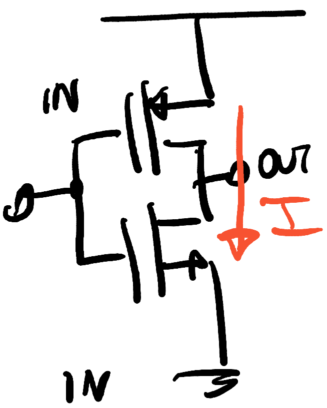
→ $\frac{1}{2} C_L V_{DD}^2$ dissipata dal pMOS.

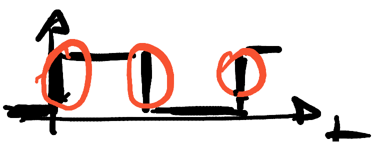
$$P_{C_L} = C_L V_{DD}^2 f$$

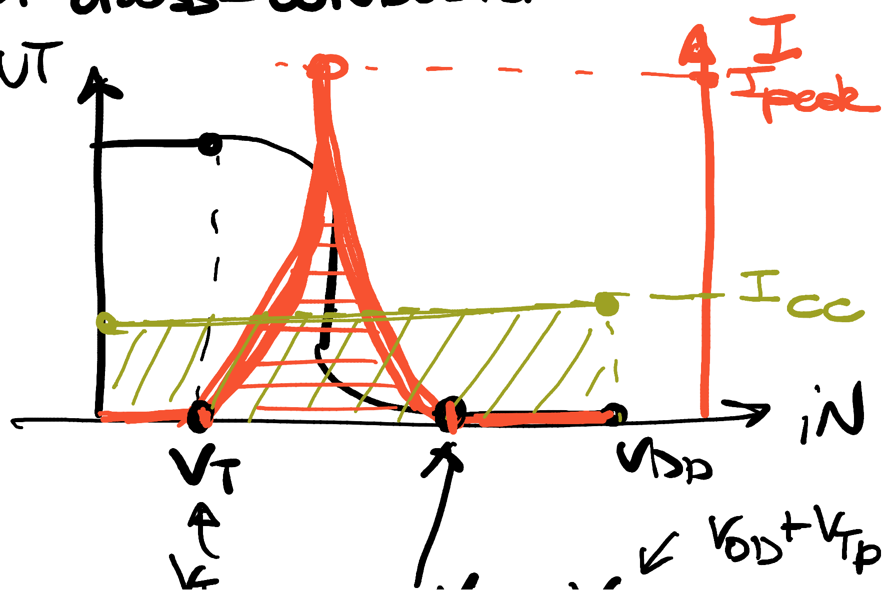
ridurre le tensioni di alimentazione (V_{DD}).

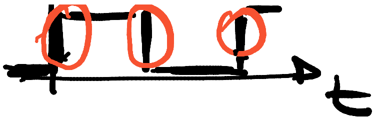
ridurre tutti i parassitismi (C_L)

POTENZA DI CROSS-CONDUZIONE









V_{Tn} ; $V_{DD}-V_T$; $V_{DD}+V_{Tp}$

$$I_{peak} = k_n (V_{GS}-V_{Tn})^2 = k_n \left(\frac{V_{DD}}{2} - V_{Tn}\right)^2 = |k_p| \left(-\frac{V_{DD}}{2} - V_{Tp}\right)^2$$

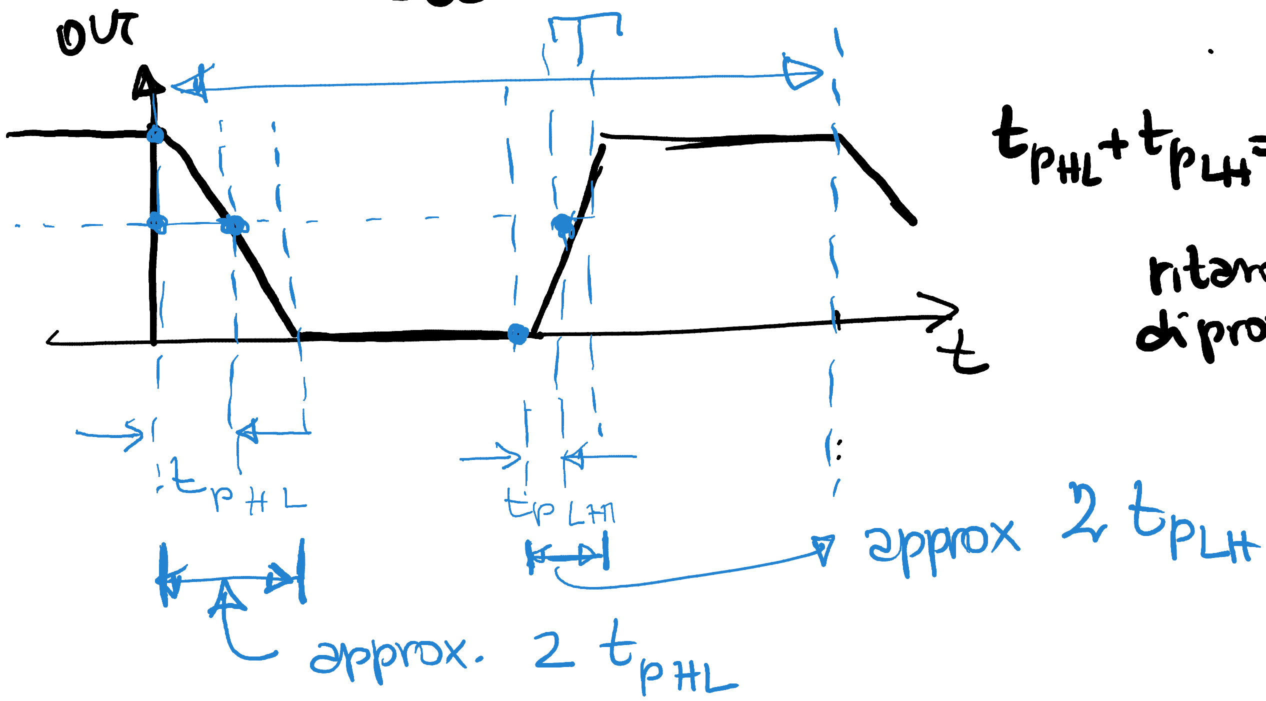
$$\overline{P_{CC}} = \overline{I_{CC}}\, V = (*)$$

$$I_{CC} = \frac{1}{2} I_{peak} \frac{V_{DD} - V_{Tn} - |V_{Tp}|}{V_{DD}}$$

corrente di cross-conduzione media

$$\frac{1}{2}(V_{DD} - V_T - V_T) * I_{peak} = I_{cc} V_{DD}$$

$$(*) = \underbrace{\left(\frac{1}{2} I_{peak} \frac{V_{DD} - 2V_T}{V_{DD}}\right)}_{I_{cc}} V_{DD} \quad \frac{2t_{pHL} + 2t_{pLH}}{T} =$$



$$t_{pHL} + t_{pLH} = 2\tau_p$$

ritardo di propag.

$$P_{cc} = \frac{1}{2} I_{peak} (V_{DD} - 2V_T)\, 2\,(2\tau_p)\, f$$

$P_{CC} = \frac{1}{2} I_{peak}$ [illegible]

$$P_{CC} \ll P_{C_L}$$

$$P_{TOT} = \cancel{P_{STATICA}}_{\simeq 0} + P_{CC} + P_{C_L}$$