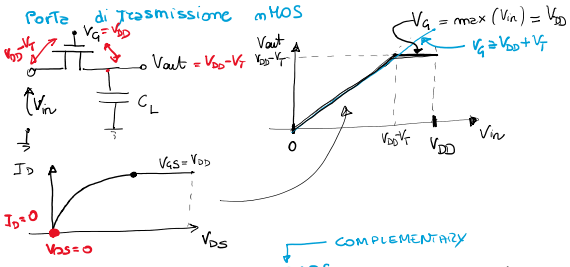
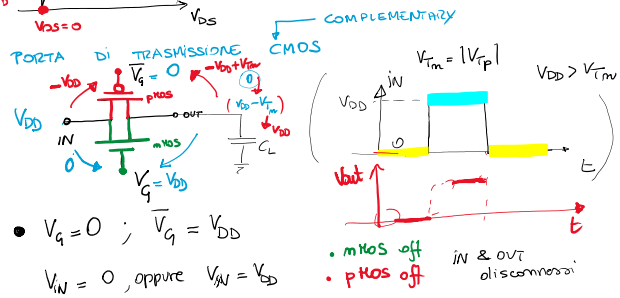
Porta di trasmissione CMOS e logica CMOS

Monday, March 15, 2021 10:54 AM





- $V_G = 0$; $\overline{V_G} = V_{DD}$

  $V_{IN} = 0$, oppure $V_{IN} = V_{DD}$

  - nMOS off
  - pMOS off

  IN & OUT disconnessi

- $V_G = V_{DD}$; $\overline{V_G} = 0$

  $V_{IN} = 0$ nMOS — lato ingresso si forma canale conduttore → nMOS on → $I_D = 0 \Rightarrow V_{DS_{nMOS}} = 0 \Rightarrow$ nMos ohmico → $V_{out} = 0$

  pMOS — lato ingresso no canale, lato uscita no canale

  ⇓

  pMOS off

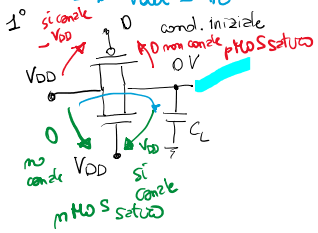
- $V_G = V_{DD}$; $\overline{V_G} = 0$

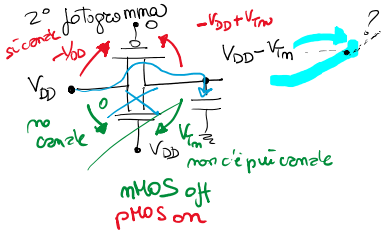
  $V_{in} = V_{DD}$

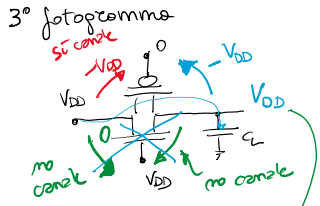
  ⇓

  $V_{out} = V_{DD}$ { fino a che Vout arriva a $V_{DD} - V_{Tn}$ la capacità è caricata da pMOS e nMOS, quando Vout arriva a $V_{DD} - V_{Tn}$, nMOS si interdice, ma il pMOS, già acceso porta $V_{out} = V_{DD}$ lavorando in zona ohmica

  → $V_{out} = V_{in}$



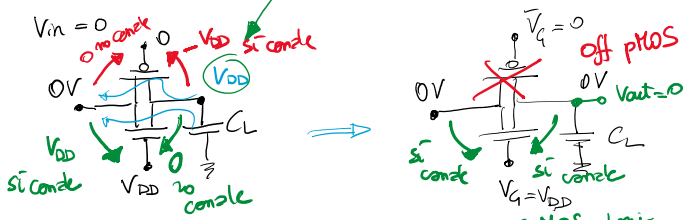




nMOS off

pMOS on in zona ohmica poichè $I_D = 0$

- $V_G = V_{DD}$; $\overline{V_G} = 0$



rispetto a una porta a singolo transistore, la porta CMOS

☺ $V_{out} = V_{in}$ anche con comando del gate pari alla dinamica di ingresso

☺ $R_{ds_{on}}$ complessivo della porta è più piccola perchè data da $R_{ds_{on_n}} \,//\, R_{ds_{on_p}}$

☹ due tensioni di comando, una negata dell'altra

PAROLA DIGITALE

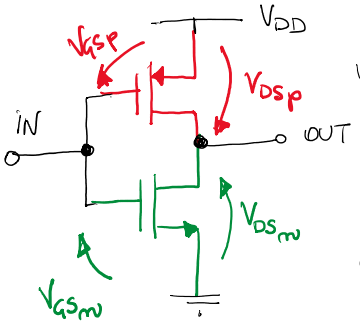
$D = [b_{N-1}, b_{N-2}, \dots, b_2, b_1, b_0]$ Parola digitale a N bit

$D = b_0 2^0 + b_1 2^1 + b_2 2^2 + \dots + b_{N-2} 2^{N-2} + b_{N-1} 2^{N-1}$

b_0: BIT MENO SIGNIFICATIVO — LEAST SIGNIFICANT BIT — LSB

b_{N-1}: BIT PIÙ SIGNIFICATIVO — MOST SIGNIFICANT BIT — MSB

INVERTER CMOS



$V_{DD} > V_T$

pMOS: $\begin{cases} V_{GSp} = IN - V_{DD} \\ V_{DSp} = V_{OUT} - V_{DD} \end{cases}$

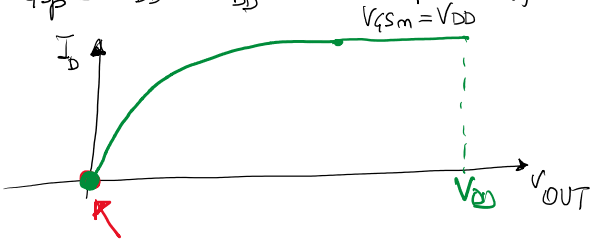
nMOS $\begin{cases} V_{GSm} = IN \\ V_{DSm} = OUT \end{cases}$

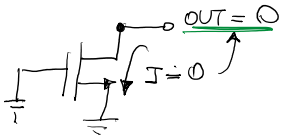
$V_T = V_{Tn} = |V_{Tp}|$

- $IN = V_{DD}$

$V_{GSn} = V_{DD} > V_{Tn} \Rightarrow$ nMOS acceso

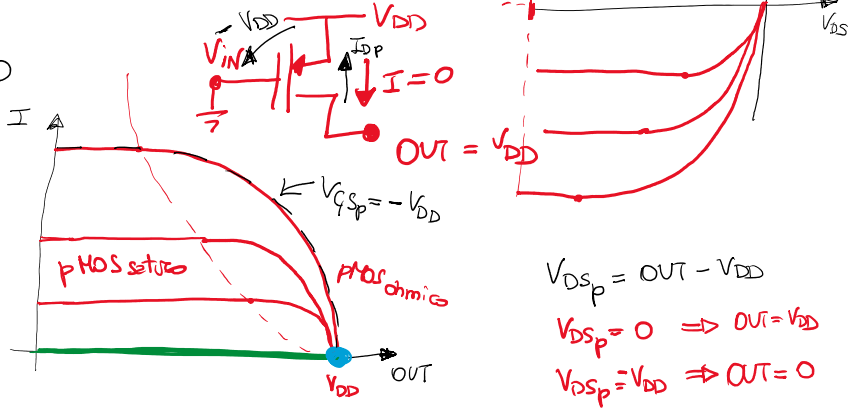
$V_{GSp} = V_{DD} - V_{DD} = 0 \Rightarrow$ pMOS off





- $IN = 0$

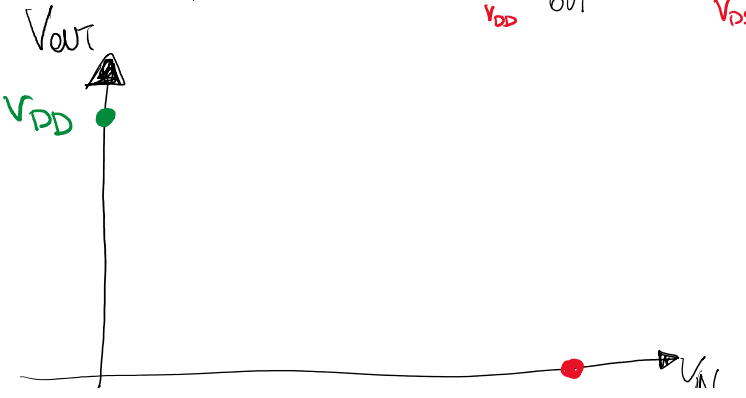
$V_{GSn} = 0$

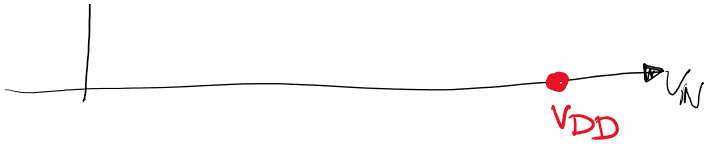


$V_{DSp} = OUT - V_{DD}$

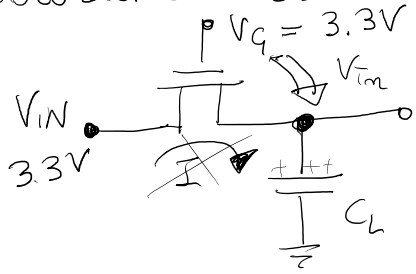
$V_{DSp} = 0 \Rightarrow OUT = V_{DD}$

$V_{DSp} = V_{DD} \Rightarrow OUT = 0$





SOLUZIONE ESERCIZIO



$V_{Tm} = 0.8V$

$V_{OUT} = 3.3V - 0.8V = 2.5V$

a) $V_{IN} = 0V$ lato ingresso $V_G - V_{in} = 3.3V \Rightarrow$ c'è canale $\Rightarrow$ MOS acceso
ma in cond. stazionarie $I = 0 \Rightarrow V_{DS_m} = 0 \Rightarrow V_{out} = V_{in} = 0V$

b) $V_{IN} = 3.3V$ lato ingresso $V_G - V_{in} = 0V \Rightarrow$ non l'è canale
ma lato uscita se $V_{out} = 0V \Rightarrow V_G - V_{out} = 3.3V > V_{Tm}$
c'è canale lato uscita, nMOS on