Logica CMOS: porte logiche complesse, porte logiche tri-state.

Monday, March 22, 2021 12:53 PM

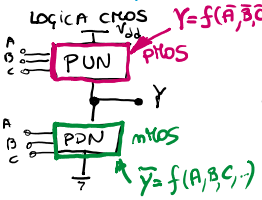
PORTE LOGICHE COMPLESSE

LOGICA CMOS $Y = f(\bar{A}, \bar{B}, \bar{C})$ OR: connessione in parallelo

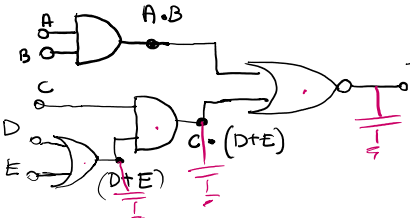
AND: connessione in serie

SOMMA DI PRODOTTI ⇒ parallelo di tanti rami con più transistori in serie

PRODOTTO DI SOMME ⇒ serie di tanti rami di 2 o più transistori in parallelo.



$$Y = \overline{A \cdot B + C \cdot (D+E)} = \overline{Y_1 + Y_2 \cdot Y_3}$$

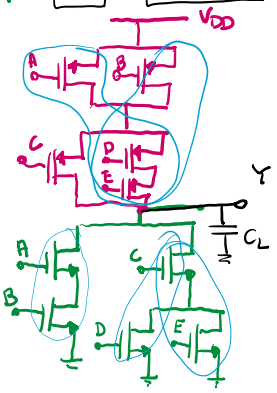


$$Y = \overline{(A \cdot B) + C \cdot (D+E)} =$$
$$= \overline{(A \cdot B)} \cdot \overline{C \cdot (D+E)} =$$
$$= (\bar{A} + \bar{B}) \cdot [\bar{C} + \overline{(D+E)}] =$$
$$= (\bar{A} + \bar{B}) \cdot [\bar{C} + \bar{D} \cdot \bar{E}]$$

PUN $Y = (\bar{A} + \bar{B}) \cdot [\bar{C} + \bar{D} \cdot \bar{E}]$

PDN $\bar{Y} = A \cdot B + C \cdot (D+E)$

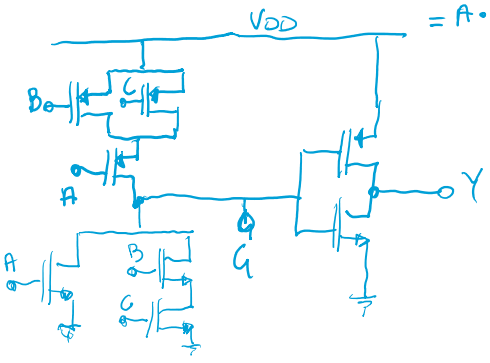
PUN
A serie D serie E
B serie D serie E

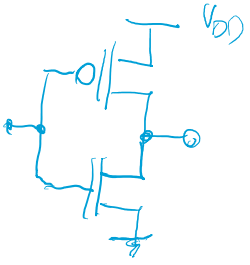


PDN
Cond. più gravose
- A serie B
- C serie D
- C serie E

$$Y = A + B \cdot C = \bar{G}$$

$$\bar{G} = A + B \cdot C \Rightarrow G = \overline{A + B \cdot C} =$$
$$= \bar{A} \cdot (\bar{B} + \bar{C})$$





Ad esempio

$$\left(\frac{W}{L}\right)_{n\,eq} = 2$$

$$\left(\frac{W}{L}\right)_{p\,eq} = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_{n\,eq} = 5 \quad \text{(per garantire inverter equivalente simmetrico)}$$

$$\left(\frac{W}{L}\right)_{eq_p} = \frac{1}{\sum_{i=1}^{3}\left(\frac{L}{W}\right)_i} = \frac{1}{3}\left(\frac{W}{L}\right)_{\substack{A,D,E \\ B,D,E}} \Rightarrow \left(\frac{W}{L}\right)_{pA} = \left(\frac{W}{L}\right)_{B_p} = \left(\frac{W}{L}\right)_{D_p} = \left(\frac{W}{L}\right)_{E_p} = 15$$

$$\left(\frac{W}{L}\right)_{p_1^C} = \frac{1}{\sum_{i=1}^{2}\left(\frac{L}{W}\right)_i} = \frac{1}{\left(\frac{L}{W}\right)_D + \left(\frac{L}{W}\right)_E} = \frac{15}{2} = 7.5$$

$$\left(\frac{W}{L}\right)_{n\,eq} = \frac{1}{2\left(\frac{L}{W}\right)_n} = \frac{1}{2}\left(\frac{W}{L}\right)_{n_{A,B,C,D,E}} \Rightarrow \left(\frac{W}{L}\right)_{n_{A,B,C,D,E}} = 4$$