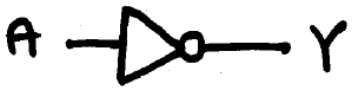
OPERAZIONI LOGICHE BOOLEANE

- **NOT**



$Y = \bar{A}$

A	Y
1	0
0	1

- **OR**

$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

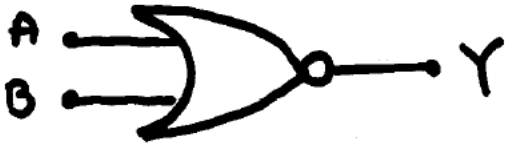
- **AND**

$Y = A \cdot B$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OPERAZIONI LOGICHE BOOLEANE

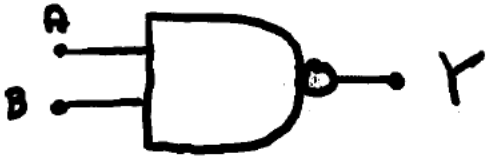
- **NOR**



$$Y = \overline{A + B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

- **NAND**

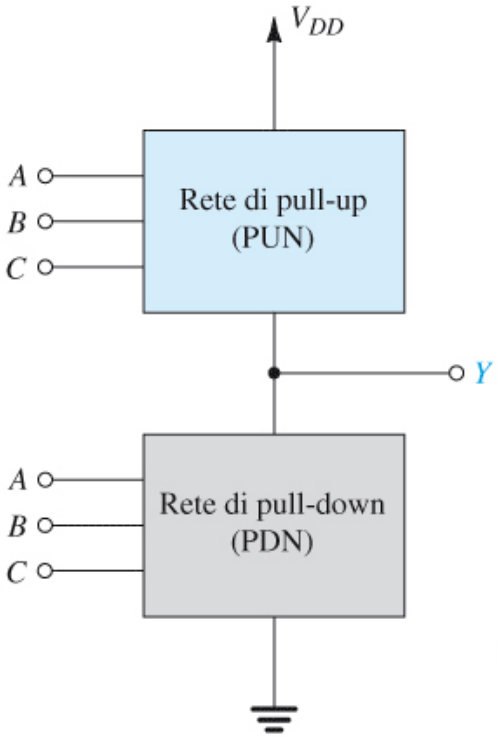


$$Y = \overline{A \cdot B}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

PORTE LOGICHE ELEMENTARI CMOS

ingressi logici



connette l'uscita all'alimentazione V_{DD}

ingressi logici

connette l'uscita a massa

Figura 14.27 Rappresentazione di una porta logica a tre ingressi. La PUN comprende transistori PMOS e la PDN comprende transistori NMOS.

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PORTE LOGICHE ELEMENTARI CMOS

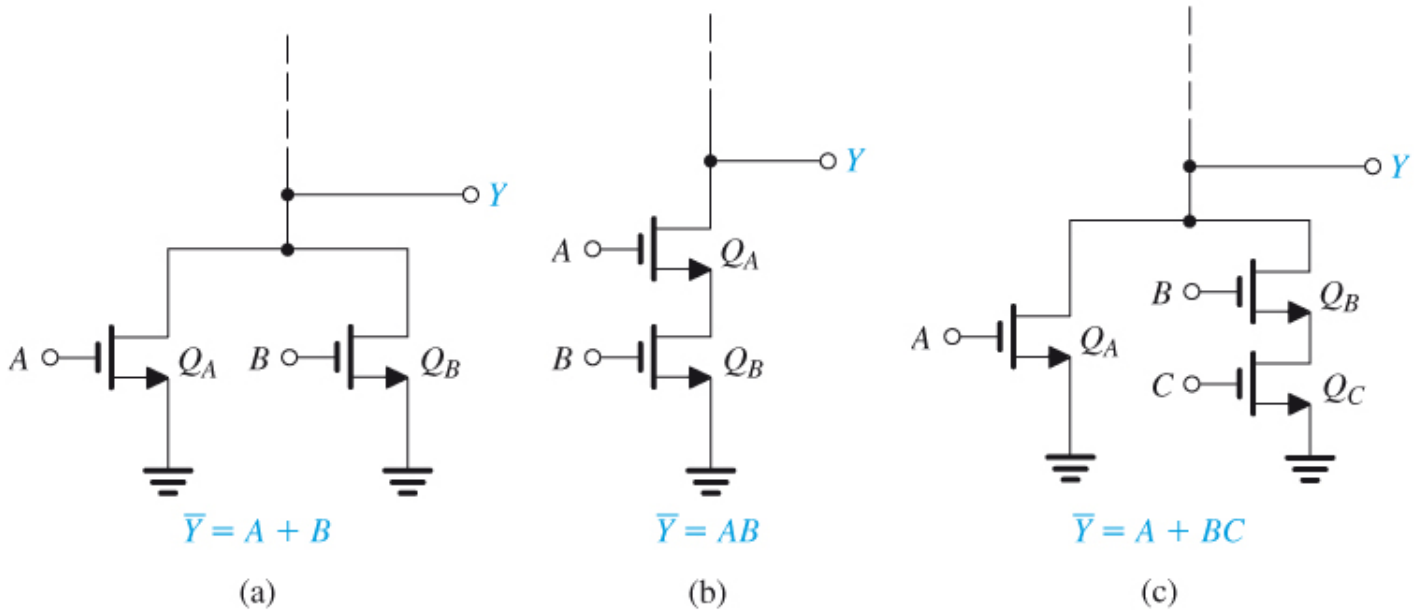

Figura 14.28 Esempi di reti di pull-down.

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PORTE LOGICHE ELEMENTARI CMOS

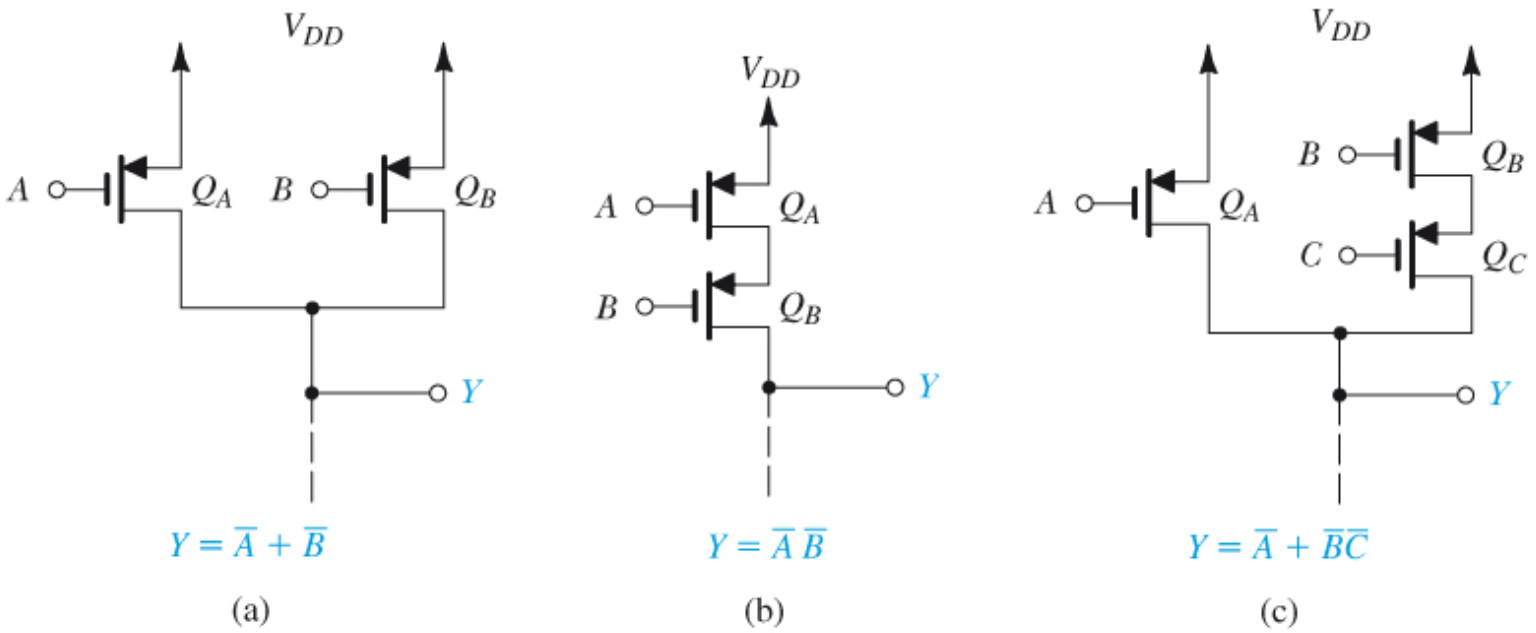

Figura 14.29 Esempi di reti di pull-up.

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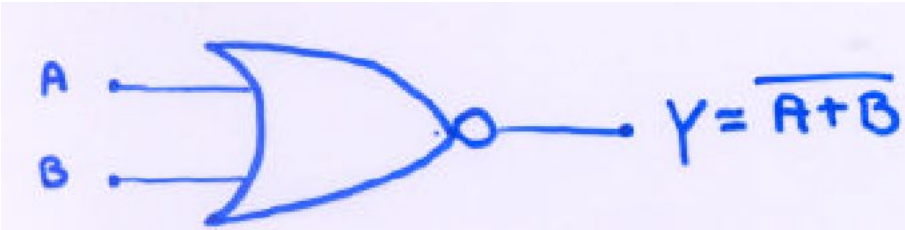
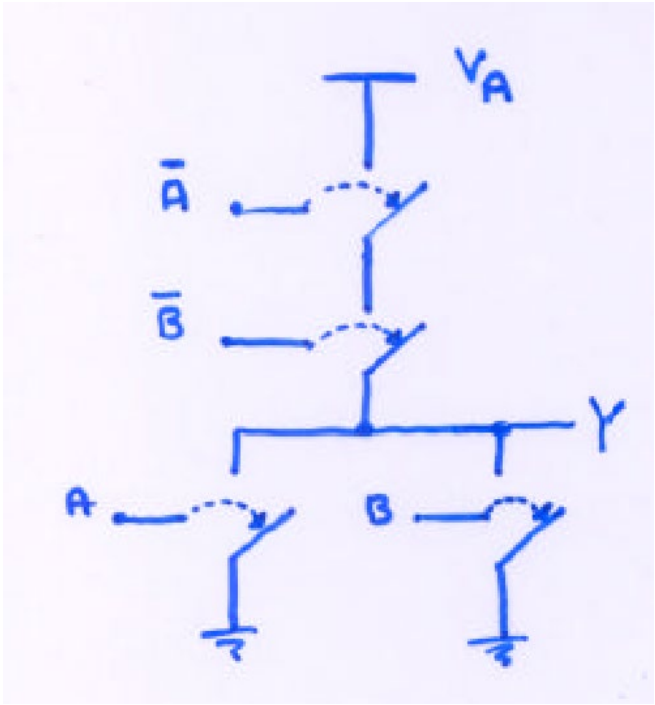
PORTA LOGICA NOR CMOS

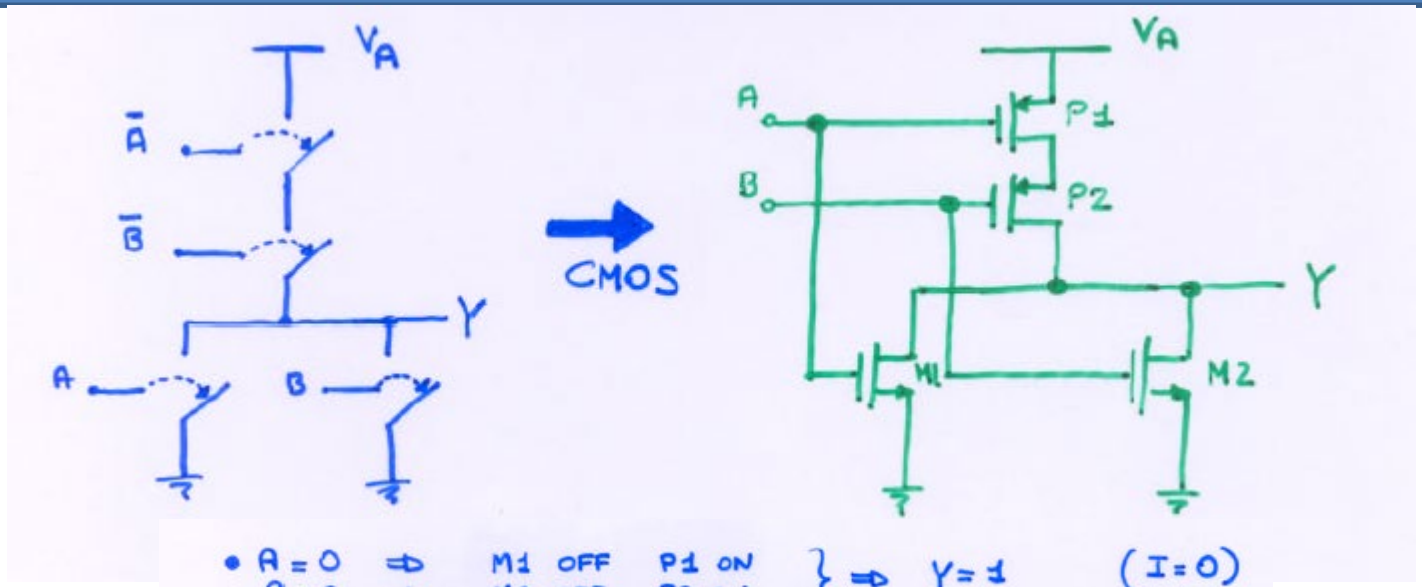


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

COME IMPLEMENTARE QUESTA TABELLA DELLE VERITA'?

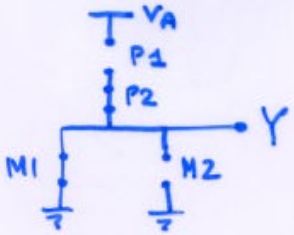


PORTA LOGICA NOR CMOS



- A = 0 ⇒ M1 OFF P1 ON
  B = 0 ⇒ M2 OFF P2 ON
  } ⇒ Y = 1 (I = 0)

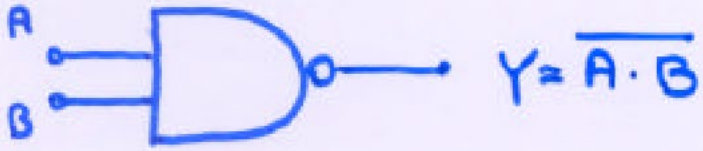
- A = 1 ⇒ M1 ON P1 OFF
  B = 0 ⇒ M2 OFF P2 ON
  } ⇒ Y = 0 (I = 0)



- A = 0 ⇒ M1 OFF P1 ON
  B = 1 ⇒ M2 ON P2 OFF
  } ⇒ Y = 0 (I = 0)

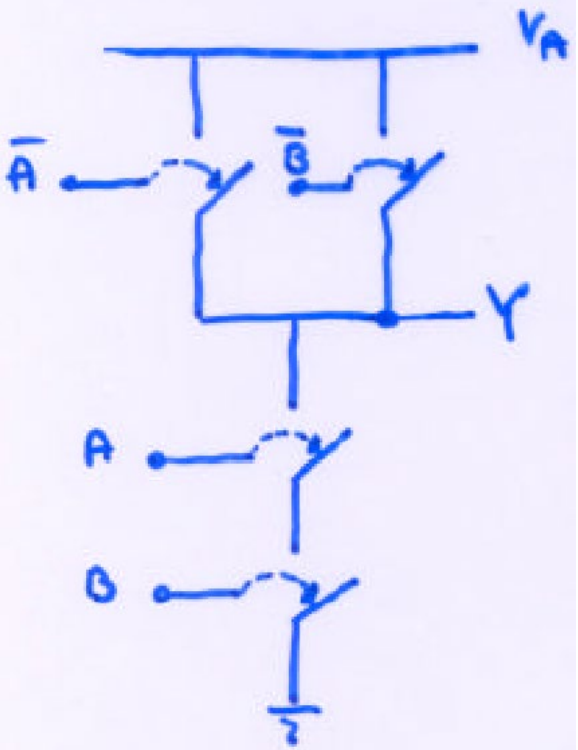
- A = 1 ⇒ M1 ON P1 OFF
  B = 1 ⇒ M2 ON P2 OFF
  } ⇒ Y = 0 (I = 0)

PORTA LOGICA NAND CMOS

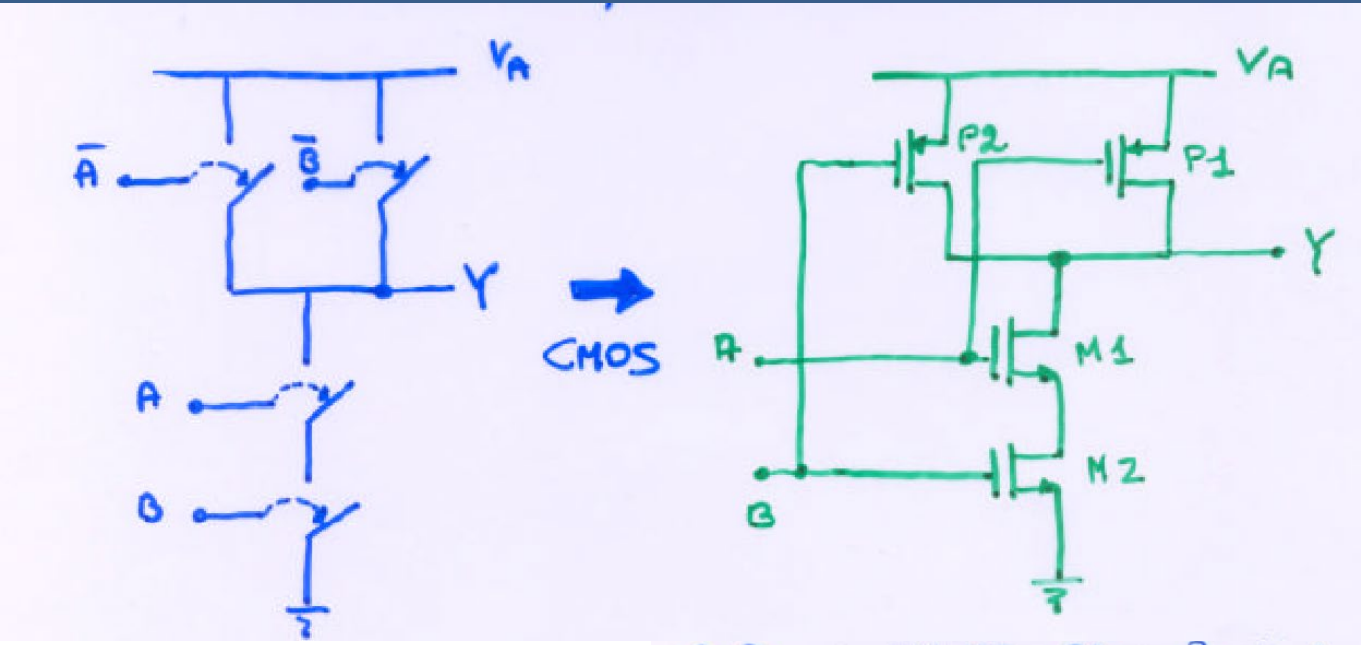


A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

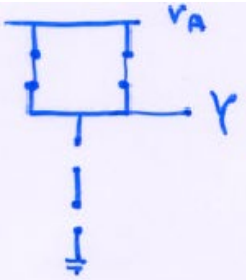
COME IMPLEMENTARE QUESTA TABELLA DELLE VERITA'?



PORTA LOGICA NAND CMOS



- A=0 ⇒ M1 OFF P1 ON
  B=0 ⇒ M2 OFF P2 ON
  } Y = 1

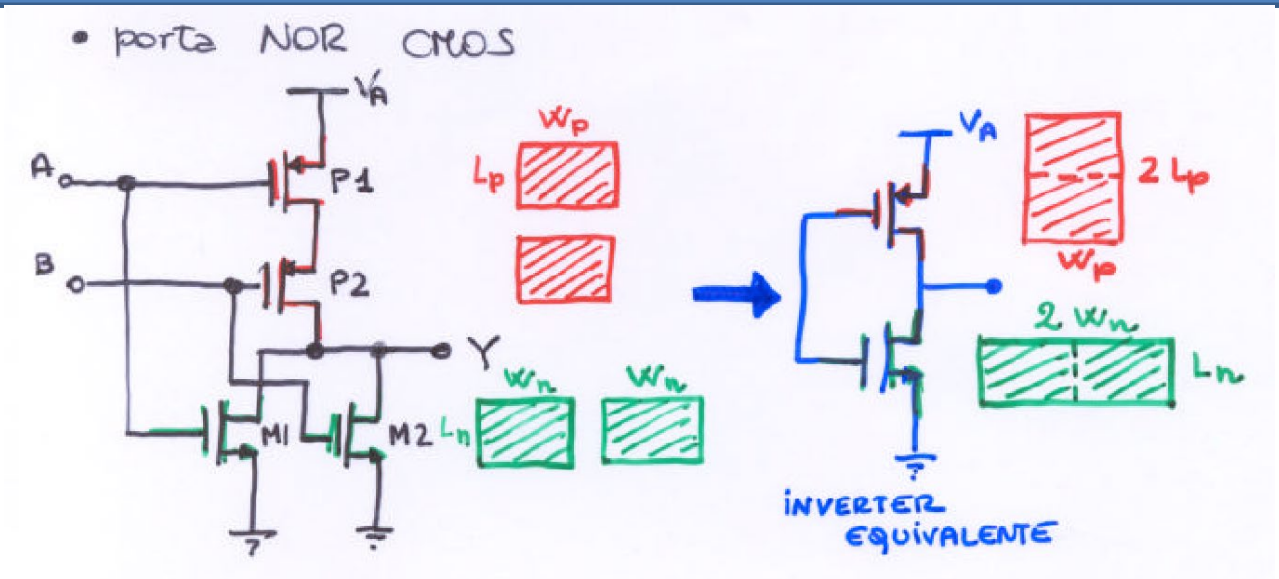


- A=1 ⇒ M1 ON P1 OFF
  B=0 ⇒ M2 OFF P2 ON
  } Y = 1

- A=0 ⇒ M1 OFF P1 ON
  B=1 ⇒ M2 ON P2 OFF
  } Y = 1

- A=1 ⇒ M1 ON P1 OFF
  B=1 ⇒ M2 ON P2 OFF
  } Y = 0

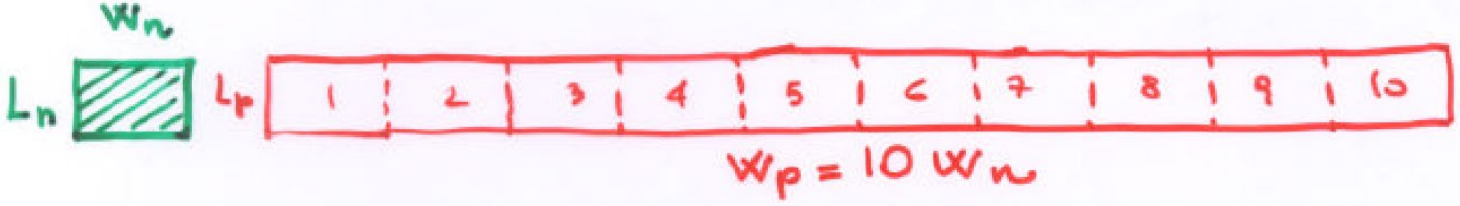
PORTA LOGICA NOR CMOS



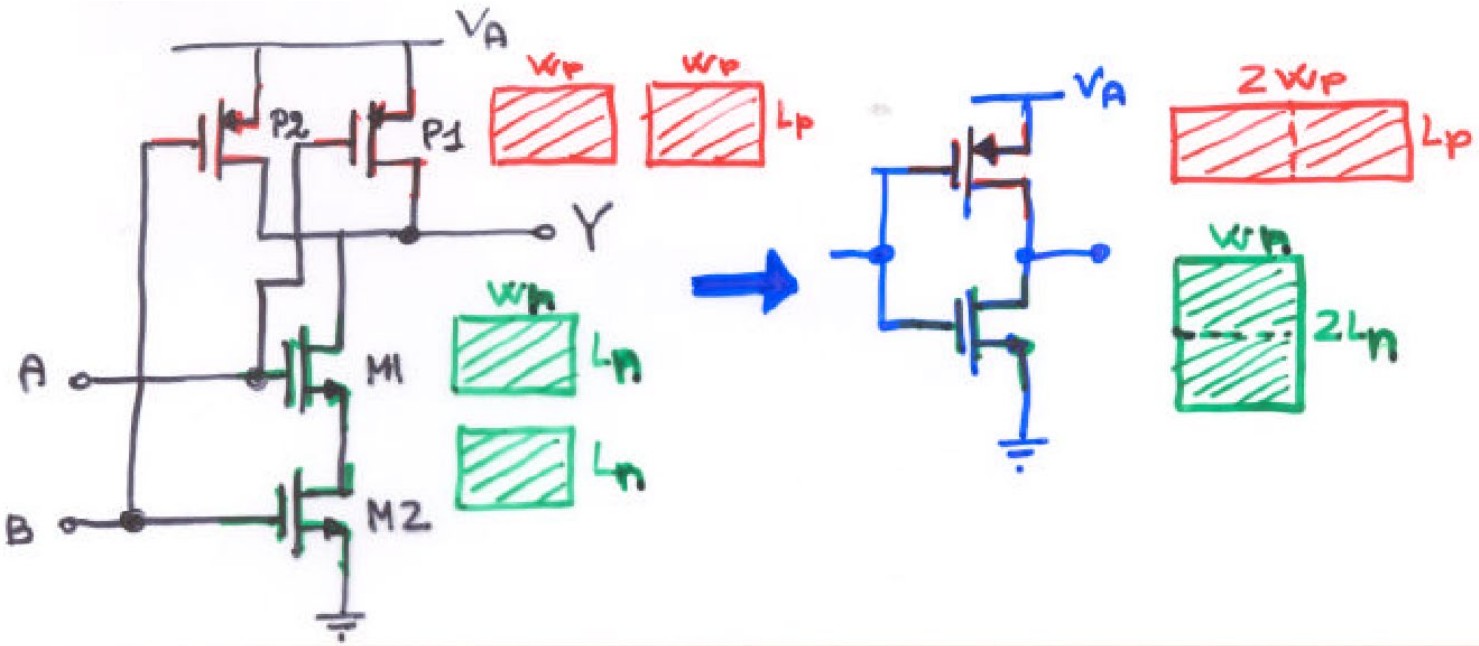
d'inverter sarà simmetrico (uguaglianza dei noise margin, uguaglianza di t_{PLH} e t_{PHL}, ...) se $k_n = |k_p|$

$$\left(\frac{W_p}{2L_p}\right) = 2.5\left(\frac{2W_n}{L_n}\right)$$

$$\left(\frac{W_p}{L_p}\right) = 10\left(\frac{W_n}{L_n}\right) \rightarrow \text{a parità di } L \quad W_p = 10\,W_n$$



PORTA LOGICA NAND CMOS



- $k_n = |k_p| \rightarrow \left(\frac{2W_p}{L_p}\right) = 2.5\left(\frac{W_n}{2L_n}\right)$

  $\rightarrow \left(\frac{W_p}{L_p}\right) = \frac{2.5}{4}\left(\frac{W_n}{L_n}\right) = 0.625\left(\frac{W_n}{L_n}\right)$

PERCHE' E' PIU' CONVENIENTE UNA LOGICA NAND CMOS DI UNA LOGICA NOR CMOS?

Assuming a symmetric equivalent inverter:

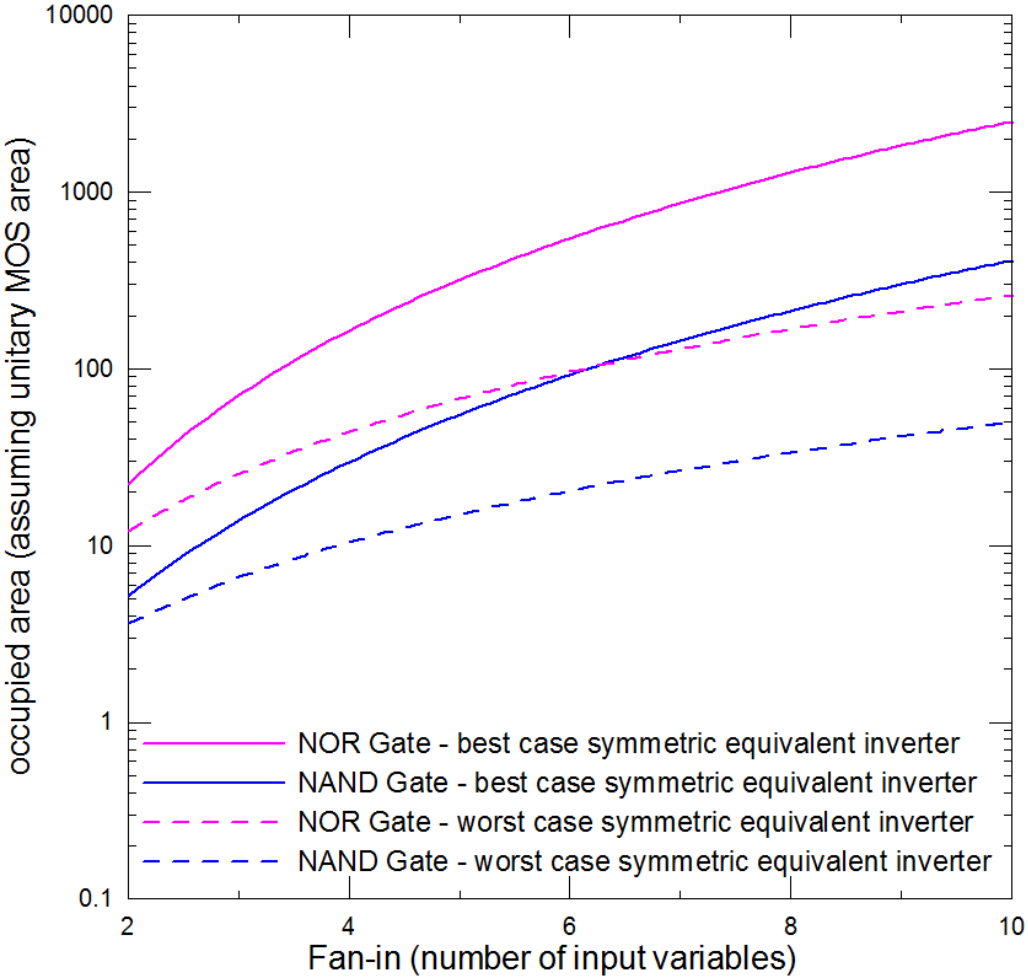
- **worst case: longest propagation time**
- **best case: shortest propagation time**

$$AREA_{NOR_{BEST\ CASE}} = AREA_{MIN} N\left(1+2.5N^2\right)$$

$$AREA_{NOR_{WORST\ CASE}} = AREA_{MIN} N\left(1+2.5N\right)$$

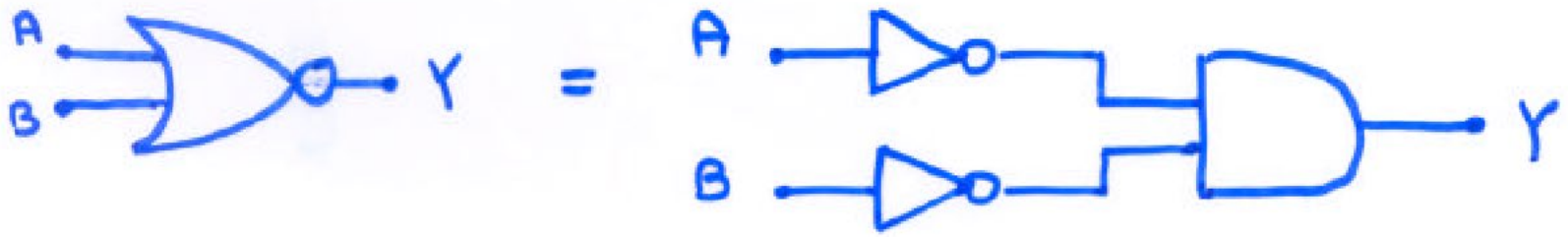
$$AREA_{NAND_{BEST\ CASE}} = AREA_{MIN} N\left(1+\frac{N^2}{2.5}\right)$$

$$AREA_{NAND_{WORST\ CASE}} = AREA_{MIN} N\left(1+\frac{N}{2.5}\right)$$

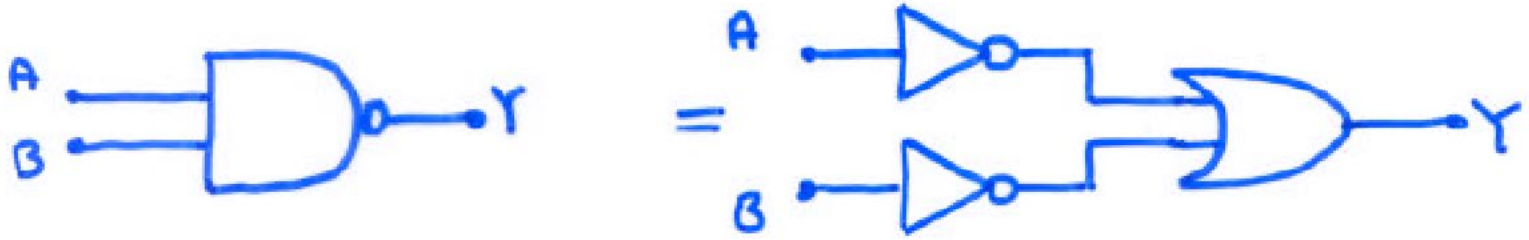


TEOREMA DI DE MORGAN

- $\overline{A+B} = \overline{A} \cdot \overline{B}$



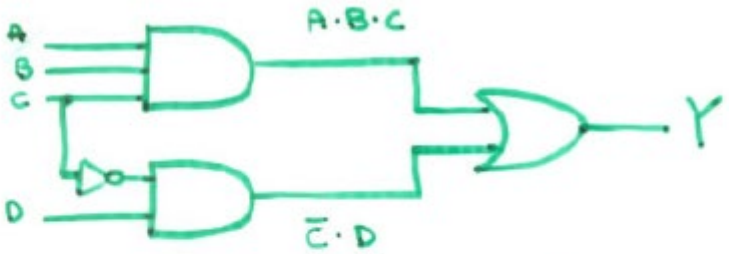
- $\overline{A \cdot B} = \overline{A} + \overline{B}$



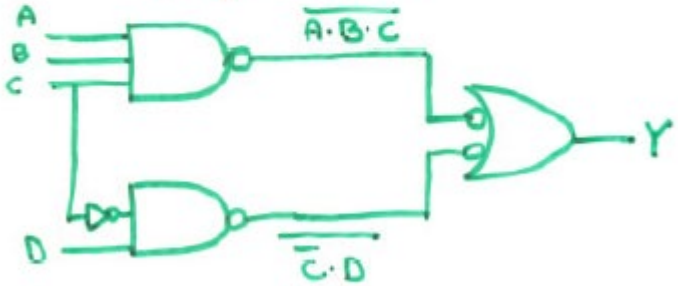
TEOREMA DI DE MORGAN

ESEMPIO DI APPLICAZIONE DEL TEOREMA DI DE MORGAN

$$Y = A \cdot B \cdot C + \overline{C} \cdot D$$

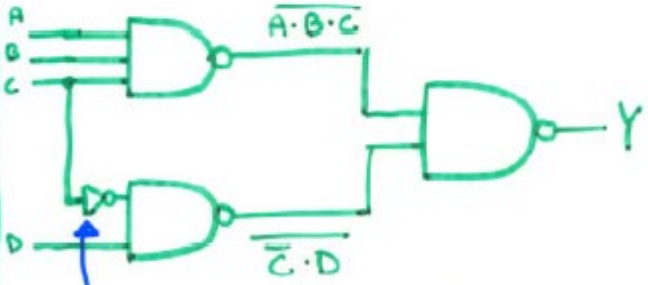


→ sostituzione porte AND con porte NAND



→ applico il Teorema di DeMorgan

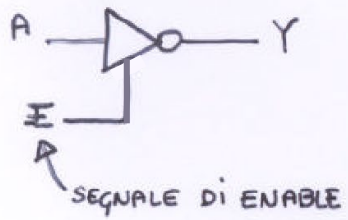
$$\overline{A} + \overline{B} = \overline{A \cdot B}$$

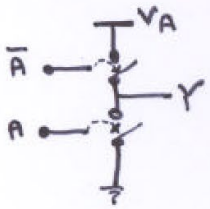


anche il NOT è realizzabile con una NAND con ingressi cortocircuitati tra loro

PORTE LOGICHE TRI-STATE

❑ SEGNALE DI ENABLE ATTIVO ALTO

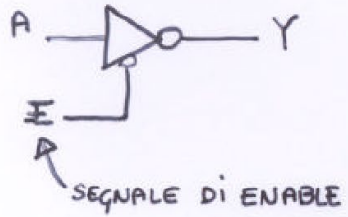


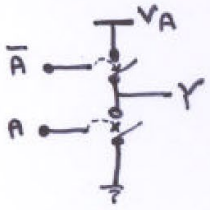


E	A	Y
1	0	1
1	1	0
0	0	High Z
0	1	High Z

è come se entrambi gli interruttori dell'inverter fossero aperti

❑ SEGNALE DI ENABLE ATTIVO BASSO



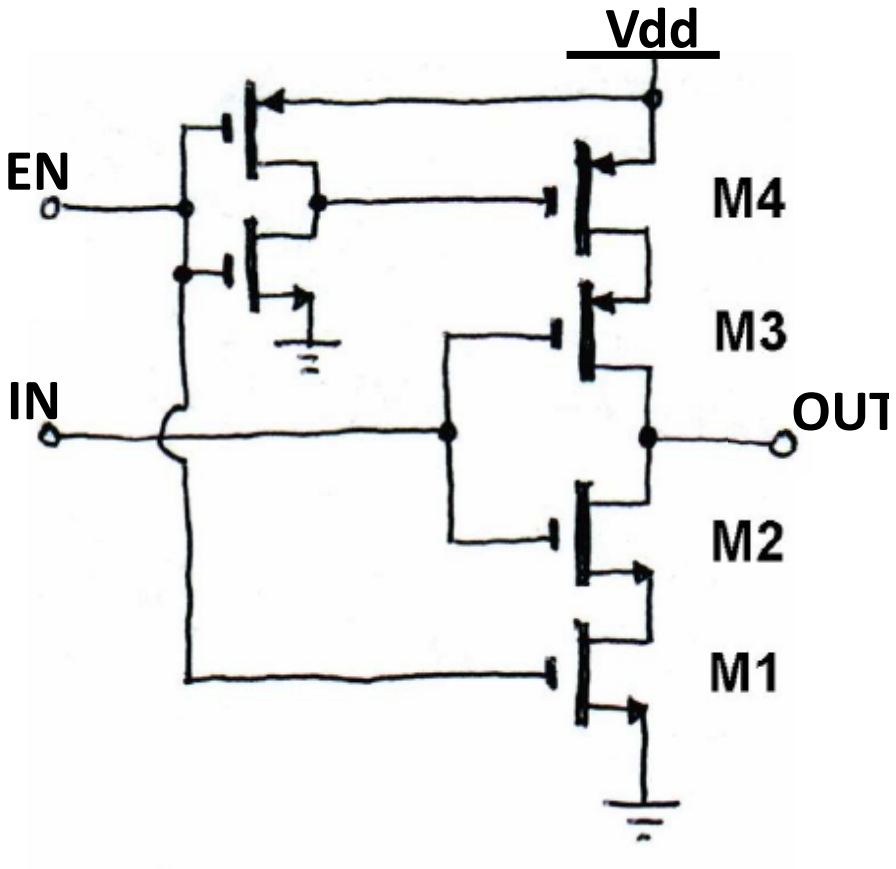


E	A	Y
0	0	1
0	1	0
1	0	High Z
1	1	High Z

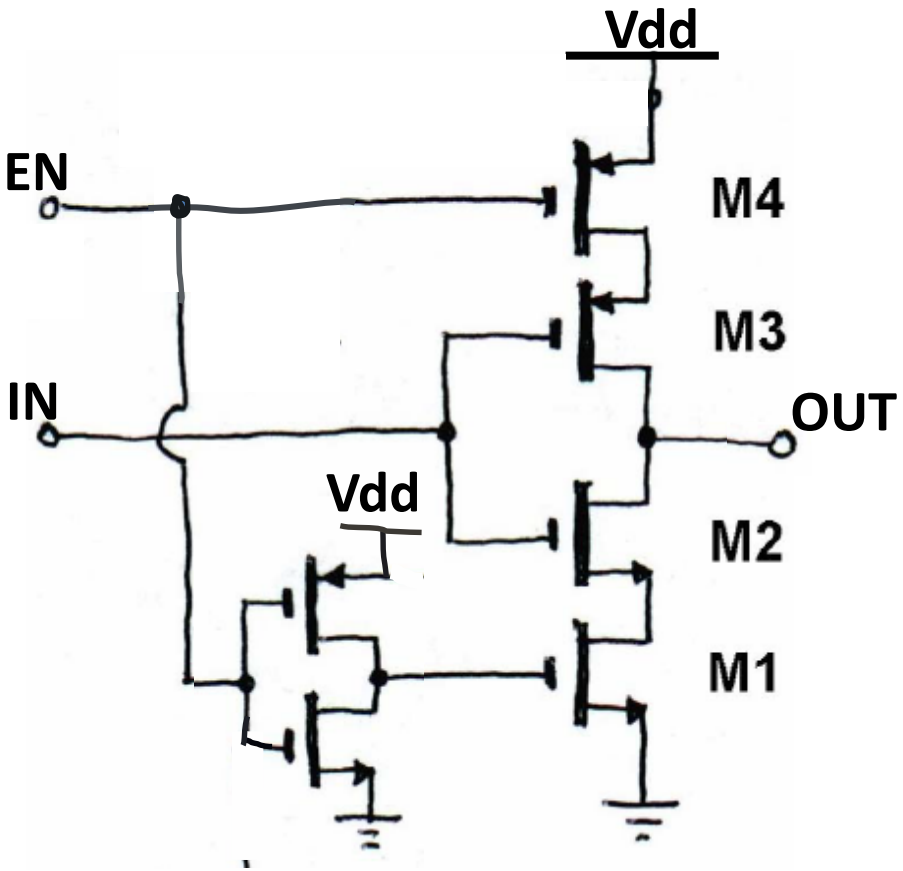
è come se entrambi gli interruttori dell'inverter fossero aperti

PORTE LOGICHE TRI-STATE

- SEGNALE DI ENABLE ATTIVO ALTO



- SEGNALE DI ENABLE ATTIVO BASSO



PORTE LOGICHE TRI-STATE

ESEMPI DI USO DELLE PORTE TRI-STATE