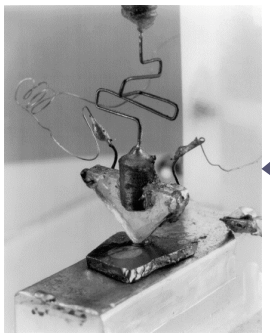
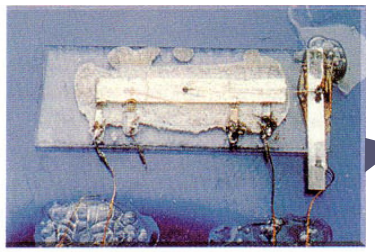
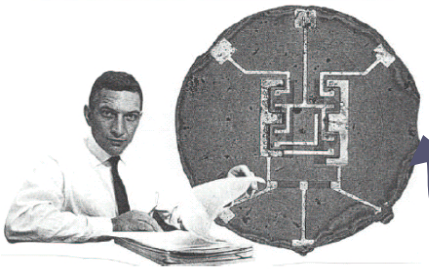
Evoluzione dei circuiti integrati



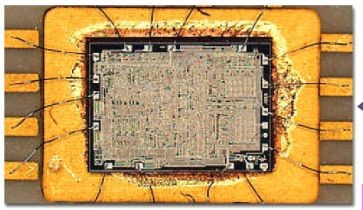
- *23 dicembre 1947,* Shockley, Brattain e Bardeen (premio Nobel per la Fisica 1956) primo transistore



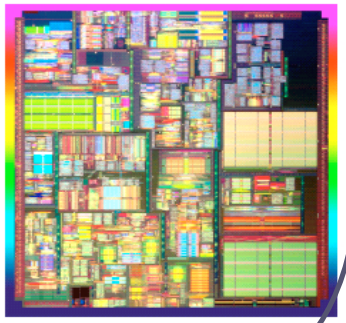
- *1958* Kilby (premio Nobel 2000 per la fisica) primo circuito integrato



- *-1959* Noyce: primo circuito integrato monolitico



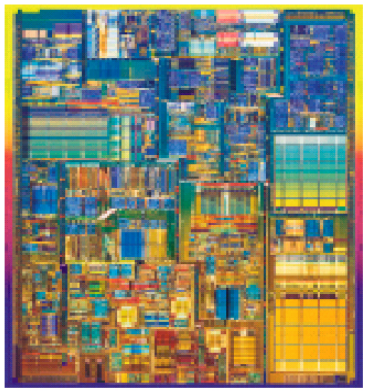
- *1970* Intel 4004
  - 2300 transistori p-MOS 8µm



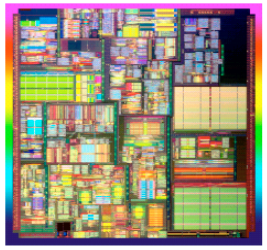
- *2000* Intel Pentium 4
  - ~50mln transistori CMOS 0.13µm

Si ringrazia l'Ing. Junior Paolo RIVA per le trasparenze

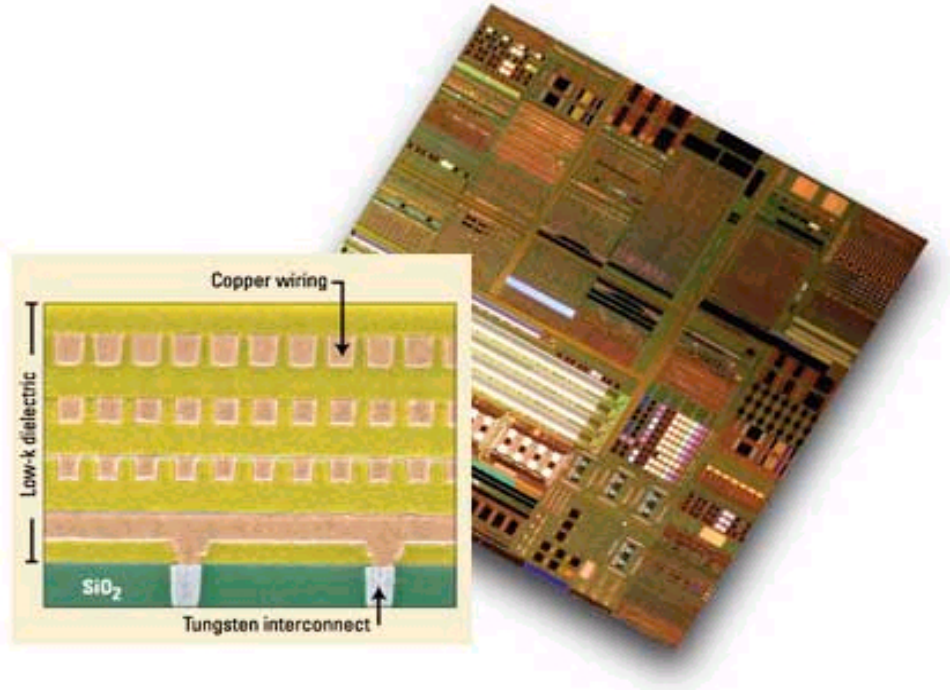
Evoluzione dei circuiti integrati



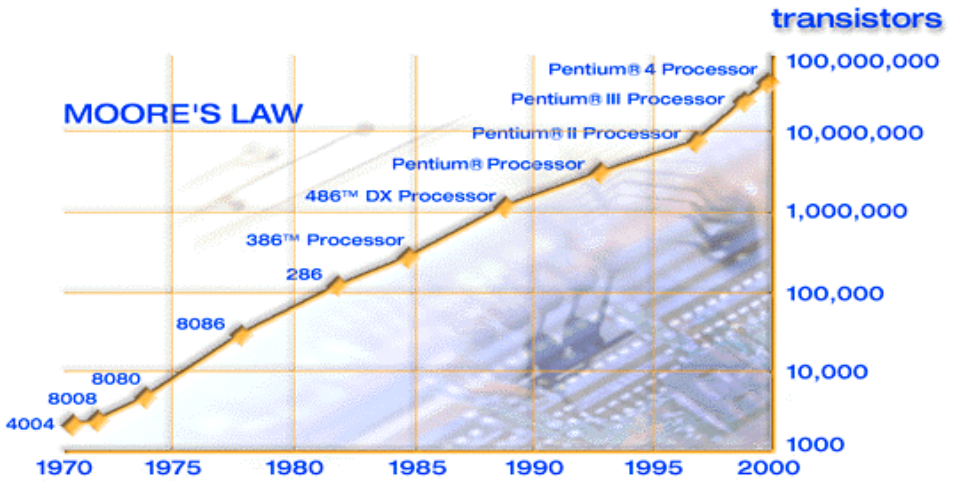
180 nm Technology



130 nm Technology

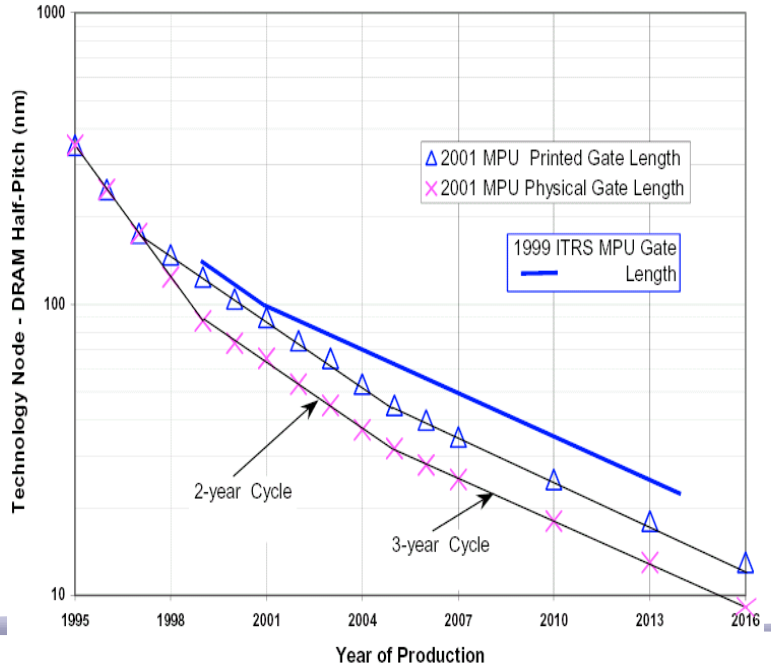


- *1998* Struttura rame dual-damascene
- *2000* Dielettrici low-k
- ASIC IBM Cu-11
  - 0.13µm Rame e SILk
  - 30% prestazioni ↑
  - 50% potenza dissipata ↓

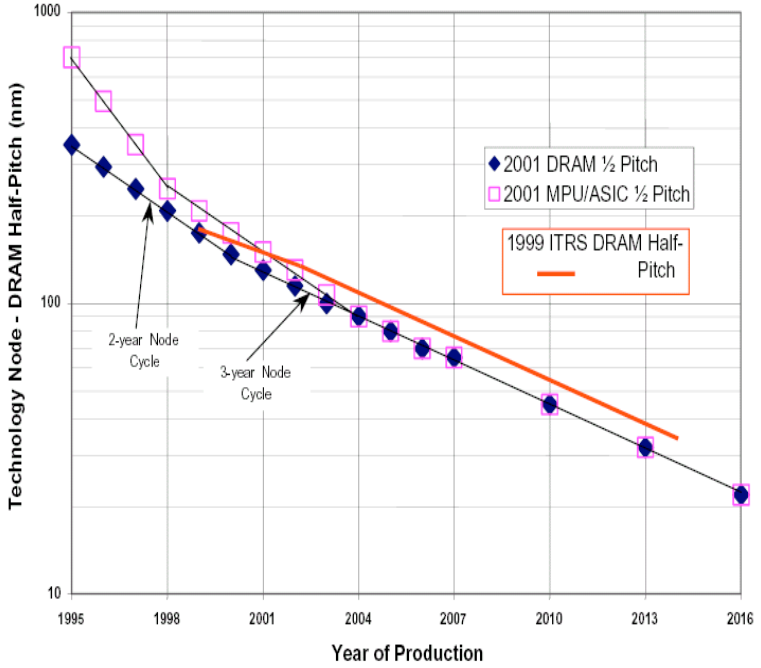


- Legge di Moore
  - N° trans/IC 2x ogni 18 mesi
  - Dim. minima 0.7x ogni 3 anni
  - Area IC 1.5x ogni 3 anni
  - Freq. Clock 1.5x ogni 3 anni
  - Costo/trans 0.5x ogni 3 anni
  - Costo Fab 2.3x ogni 3 anni
- ITRS Roadmap

ITRS Roadmap Acceleration Continues...Gate Length



ITRS Roadmap Acceleration Continues...Half Pitch



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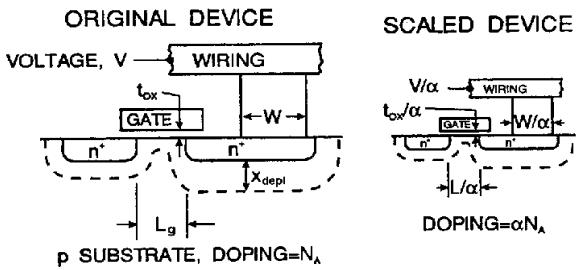

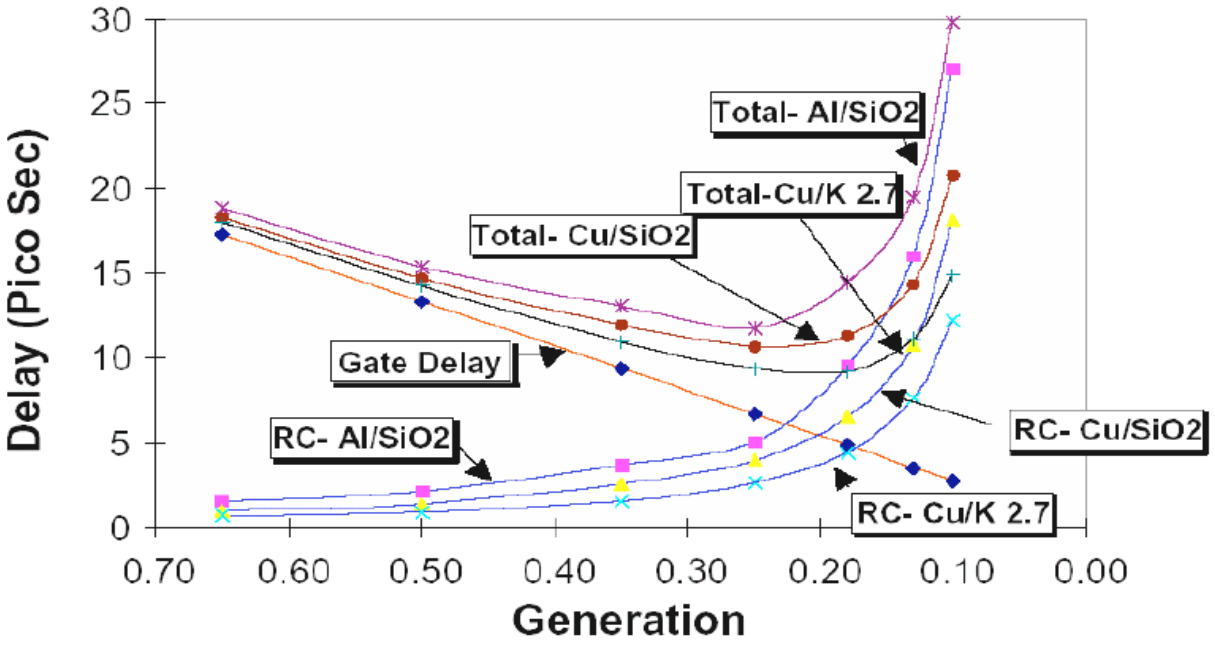

- Miglioramento prestazioni:
  - Scaling
- Ritardo RC:
  - Ritardo di gate ↓
  - Ritardo delle interconnessioni ↑
- Soluzioni per limitare il ritardo:
  - Rame
  - Dielettrici *low-k*