SUPERPOSITION THEOREM

The superposition Theorem is applicable ONLY to linear networks.

- It states that the response (Voltage or Current) in any branch of the linear circuit having more than one INDEPENDENT source equals the algebraic sum of the responses caused by each independent source acting alone, while all other independent sources are replaced by their internal impedances.

To ascertain the contribution of each individual source, all of the other independent sources first must be "turned off" (i.e. set to zero) by:

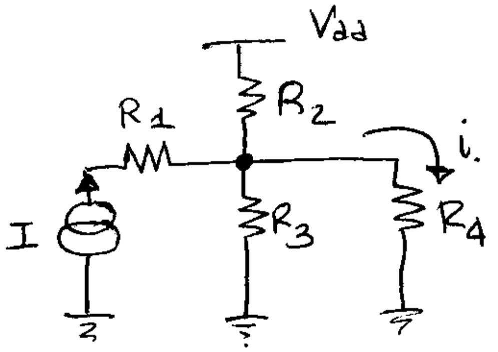
- replacing all other independent voltage sources with a short circuit (~~ideal~~ internal impedance of an ideal voltage source is zero)
- replacing all other independent current sources with an open circuit (internal impedance of an ideal current source is infinite)

This procedure is followed for each source in turn, then the resultant responses are added to determine the true operation of the circuit. The resultant circuit operation is the superposition of the various voltage and current sources.

- It is applicable to LINEAR NETWORKS (TIME VARYING or TIME INVARIANT) consisting of independent sources, linear dependent sources, linear elements (resistors, inductors, capacitors) and linear transformers

EXERCISE

Let's consider The following circuit:



$V_{dd} = +5V$ $\quad I = 2mA$

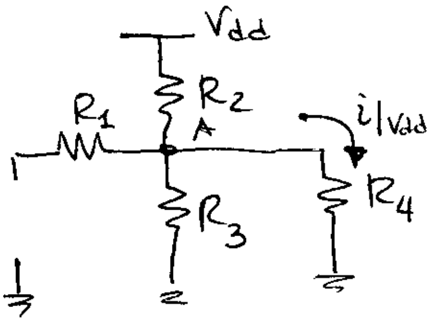
$R_1 = 400k\Omega$ $\quad R_4 = 10k\Omega$

$R_2 = 500k\Omega$

$R_3 = 100k\Omega$

1. Let's calculate The current i flowing in The resistor R_4
2. Let's suppose To measure That current i with an amperometer with an internal resistance equal to 500Ω.
   Which is The True measured current? Which is The voltage drop across The amperometer?

1. The circuit is linear, Therefore we can apply The superposition Theorem.
   Let's switch off The current generator I ⇒ it will be substituted by an open circuit



The current flowing in resistor R_2 is

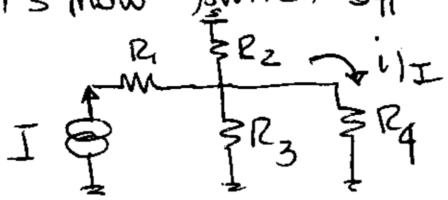
$$i_{R_2}\Big|_{V_{dd}} = \frac{V_{dd}}{R_2 + R_3 /\!/ R_4} = 9{,}82\,\mu A$$

By applying The current divider law at node A we find:

$$i\Big|_{V_{dd}} = i_{R_2}\Big|_{V_{dd}} \cdot \frac{R_3}{\underbrace{R_3 + R_4}_{\text{sum of The resistances of The Two branches}}} = 8{,}93\,\mu A$$

← resistance in which current doesn't flow

Let's now switch off The voltage generator V_{dd}



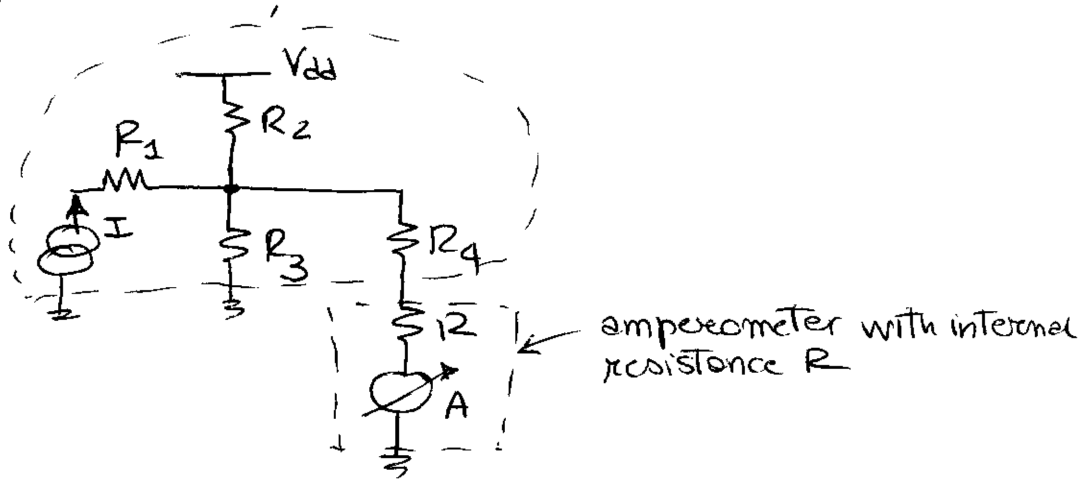
current divider law

$$i_I = I \, \frac{R_2 /\!/ R_3}{R_2 /\!/ R_3 + R_4} = 1.8\,mA$$

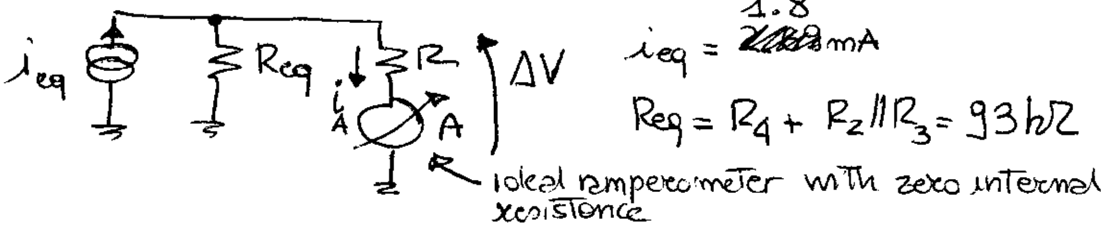
↳ by summing The Two contributions:

$i = i|_I + i|_{V_{dd}} = 1.8\,mA + 8{,}93\,\mu A = 1{,}8\,mA$

2. An amperometer can be modeled as an ideal amperometer (i.e. with no internal resistance and therefore with voltage drop at its terminals equal to zero) with a series resistor of $R = 500\,\Omega$, in our case



Let's compute the Norton equivalent of the highlighted network. The "short circuit current is the one found before



$i_{eq} = 1.8\,\text{mA}$

$R_{eq} = R_4 + R_2 /\!/ R_3 = 93\,k\Omega$

$$\Downarrow \quad i_A = \frac{R_{eq}}{R + R_{eq}}\, i_{eq} = \frac{93\,k\Omega}{93.5\,k\Omega} * 1.8\,\text{mA} = 1.79\,\text{mA}$$

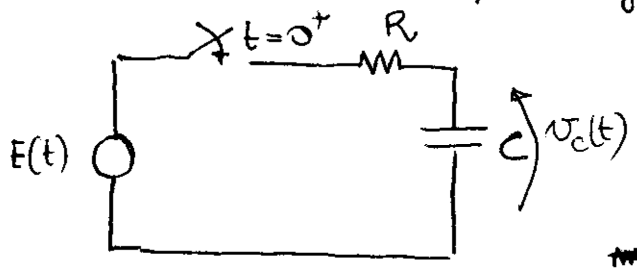
$\Delta V = i_A * R = 0.89\,V$!! instead of the ideal 0 V drop.

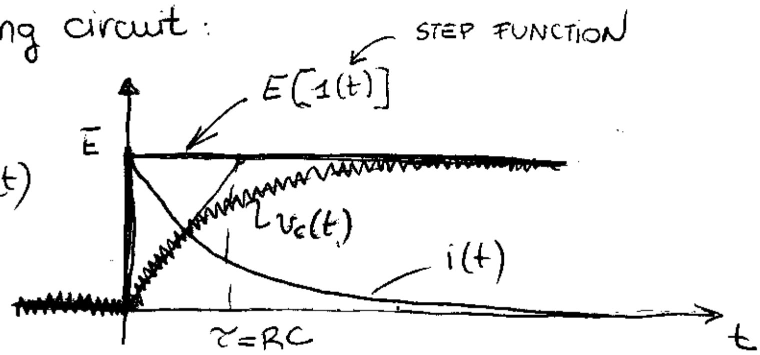
RC CIRCUIT IN THE TIME DOMAIN

- The time evolution of a linear network with lumped elements is governed by a set of ~~linear~~ ordinary differential equations with constant coefficients and of order equal to the number of independent reactive elements present in the network.

- Capacitors (and inductors) are dependent when they can be reduced to a single element (series, parallel) or when their energetic condition is set by a condition (e.g. three capacitors on the three sides of a loop)

- Let's consider the following circuit:





- Let's consider the capacitor C initially uncharged
  ↳ $Q=0 \Rightarrow v_c(t)=0$

- at the beginning of the the transient the current flowing in the resistor R is equal to

$$I = \frac{E}{R} = \frac{Q}{t}$$

and therefore it charges the capacitor by accumulating the charge $Q = \frac{E}{R}t$ on its plates.

↳ $v_c(t) \simeq \frac{Q(t)}{C} \simeq \frac{E}{RC}t$ for $t \ll RC$

- The voltage across the capacitor varies with time, therefore also the current flowing in the resistor R varies with time
  ↳ the current charging the capacitor becomes smaller and smaller and the voltage across the capacitors builds up

more slowly, until the voltage across the resistor becomes zero and, therefore, also the charging current

↳ v_c reaches the voltage E and saturates at that value.

⇩

Differential equation

$$v_c(t) = E - R\,i(t) = E - RC\,\frac{dv_c(t)}{dt}$$

⇩

$$v_c(t) = E\left[1 - \exp\left(-\frac{t}{RC}\right)\right] \underset{t \ll \tau}{\simeq} E\,\frac{t}{\tau} \qquad \tau = RC$$

$\tau = RC$ ← RC CIRCUIT TIME CONSTANT

- RISE-TIME: time needed for the output voltage to go from 10% of its final value to 90% of it.

$$t_{rise_{10-90\%}} = 2.2\,\tau$$

- $t > 5\tau \Rightarrow \dfrac{E - v_c(t)}{E} < 1\%$

⇩ in order to know the time evolution of the network for SINGLE TIME CONSTANT CIRCUITS (circuits composed of, or that can be reduced to, one reactive component and one resistor) it is enough to know the circuit time constant τ, the initial value of the output variable and the final value. The connection between the initial value and the final value is exponential with single time constant equal to the circuit time constant

METHOD OF ANALYSIS OF SINGLE TIME CONSTANT CIRCUITS

1. Evaluate The Time constant τ

   a. reduce excitation to zero
      - voltage source → short it
      - current source → open it

   b. find The equivalent resistor in parallel to The capacitor (or The equivalent capacitor in parallel To The resistor)

      * one single capacitor:
        - take out The capacitor
        - compute The equivalent resistors at The capacitor Terminals (R_{eq})

        ↳ $\tau = C R_{eq}$

      * more dependent capacitors:
        - take out The resistance
        - find The equivalent capacitor at The Terminals of The resistor (C_{eq})

        ↳ $\tau = R C_{eq}$

      * more Than one resistor and more Than one capacitor

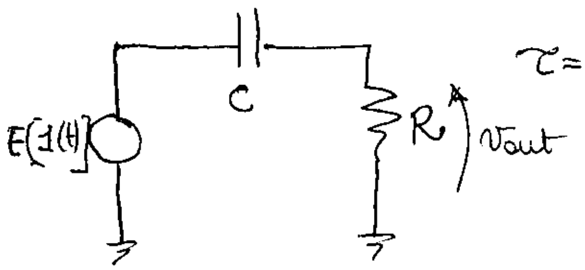
        ↳ initial work to simplify The circuit

2. Compute The output variable at $t \to \infty$ → The input source is nearly constant → The capacitor does not let any current to flow Through it (i.e. open circuit)

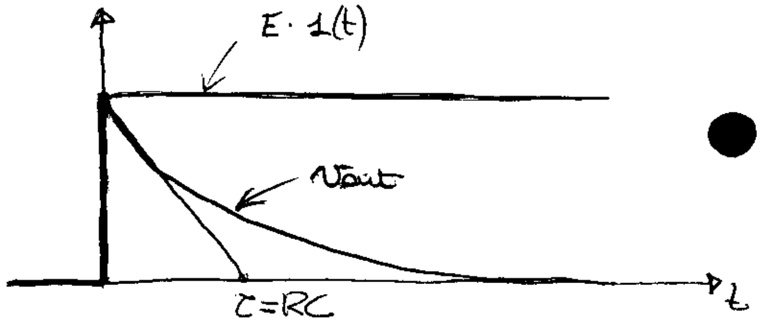
3. Compute The output variable at $t = 0^+$ → on The edge of The transition, The capacitor cannot change The voltage across its Terminals → it acts as a voltage source with The voltage difference of $t = 0^-$:

4. Connect The initial value and The final value with an exponential function with single Time constant equal to τ.

a/ CR CIRCUIT



$\tau = RC$



$t = 0^+$: The capacitor cannot change the voltage drop at its terminal instantaneously

$\hookrightarrow \Delta V_c(0^-) = 0 = \Delta V_c(0^+)$

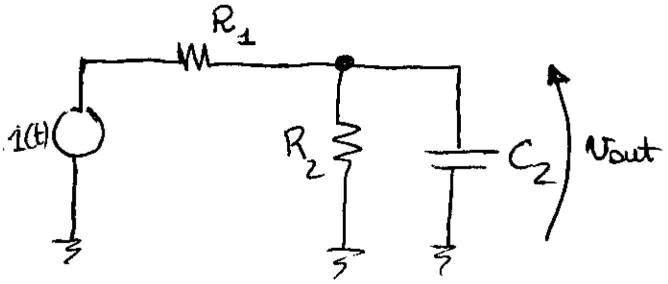
$\Downarrow$

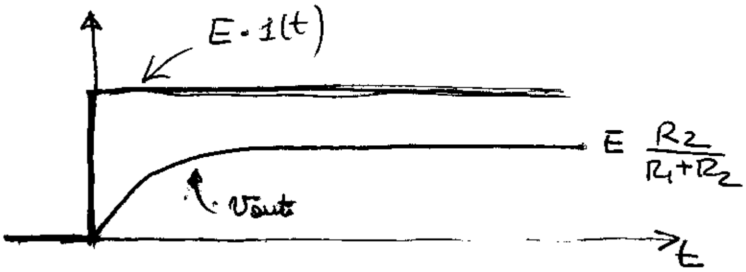
$v_{out}(t = 0^+) = E$

$t > 0^+$: The capacitor is charged by the transient current flowing in the loop

$t \to \infty$ The capacitor acts as an open circuit $\Rightarrow i = 0$; $v_{out} = 0$

EXERCISE



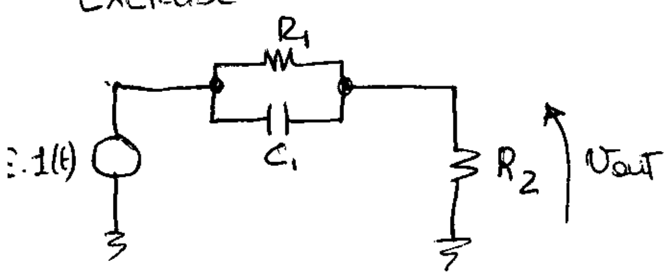


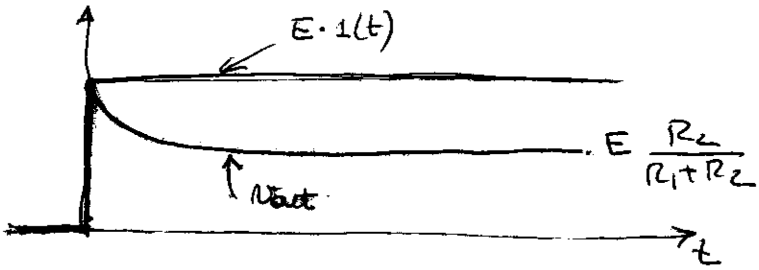
$t = 0^+$: $\Delta V_c(0^-) = 0 = \Delta V_c(0^+) \Rightarrow v_{out}(0^+) = 0$

$t \to \infty$ C_2 open circuit $\Rightarrow v_{out} = \frac{R_2}{R_1 + R_2} E$

$\tau = C_2 * R_{eq} = C_2 (R_1 /\!/ R_2)$

EXERCISE



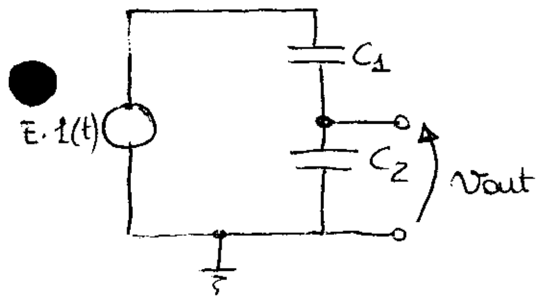


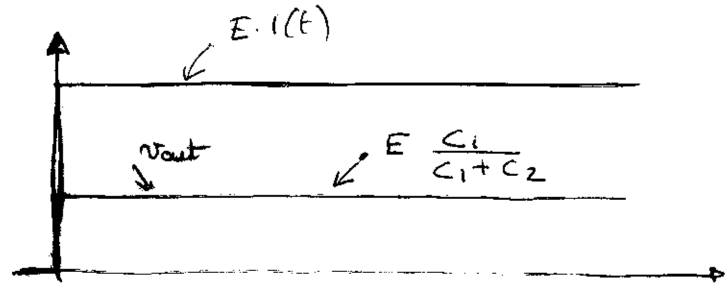
$\tau = C_1 * R_{eq} = C_1 (R_1 /\!/ R_2)$

$t = 0^+$ $\Delta V_c(0^-) = 0 = \Delta V_c(0^+) \Rightarrow v_{out}(0^+) = E$

$t \to \infty$ C_1 open circuit $\Rightarrow v_{out} = \frac{R_2}{R_1 + R_2} E$

CAPACITIVE DIVIDER





C_1 and C_2 are in series

↳ $i_1 = i_2 \rightarrow C_1 \frac{dv_1}{dt} = C_2 \frac{dv_2}{dt}$

$$\Downarrow \frac{C_1}{C_2} = \frac{dv_2}{dv_1} \rightarrow dv_2 = \frac{C_1}{C_2} dv_1$$

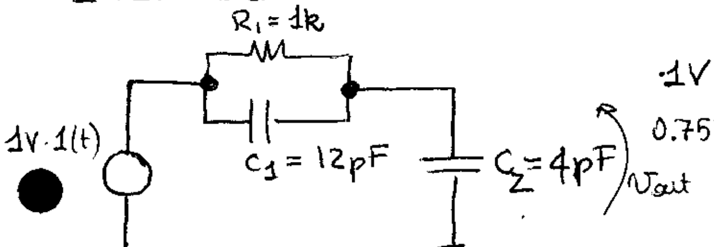
By integrating

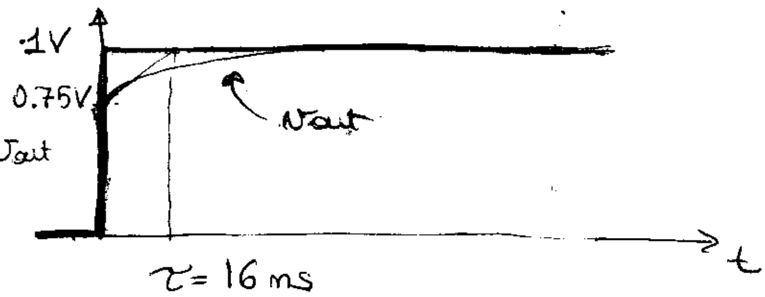
$$v_2 = \frac{C_1}{C_2} v_1 = \frac{C_1}{C_2}(E - v_2) = E\frac{C_1}{C_2} - \frac{C_1}{C_2} v_2$$

$$\Downarrow$$

$$v_{out} = v_2 = E \frac{C_1/C_2}{1 + \frac{C_1}{C_2}} = E \frac{C_1}{C_1 + C_2}$$

EXERCISE





$t = 0^+$: at the step the capacitors are dominating the behaviour of the network ⇒ capacitive divider

$$v_{out}(0^+) = \frac{C_1}{C_1 + C_2} 1V = \frac{12pF}{16pF} 1V = 0.75V$$

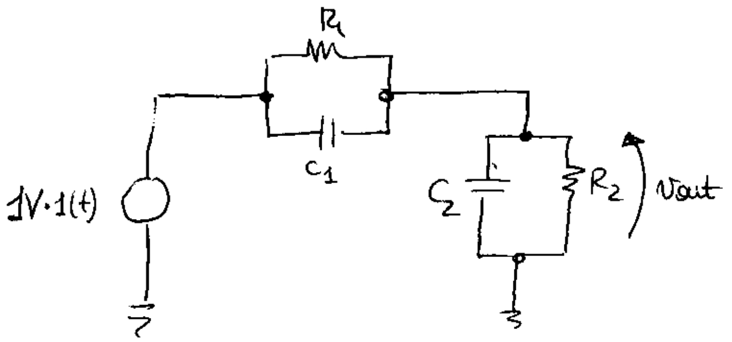
$t \to \infty$: C_1 and C_2 are open circuits → in R_1 no current can flow

↳ $v_{out} = 1V$

τ : The capacitors C_1 and C_2 are dependent (if we fix the charge deposited on the plates of one of the two and hence its voltage drop, the charge stored in the second is automatically set)

C_1 and C_2 are in parallel ⇒ $\tau = (C_1 + C_2) R_1 = 16$ ms

8/ COMPENSATED DIVIDER



$R_1 = 1k\Omega$

$R_2 = 1k\Omega$

$C_1 = 12pF$

$C_2 = 4pF$

τ: The two capacitors are in parallel $\Rightarrow$ single time constant

$$\tau = (R_1 \| R_2)(C_1 + C_2) = (1k \| 1k)(12pF + 4pF) = 8ns$$

$t = 0^+$: The capacitors dominates the behaviour of the network

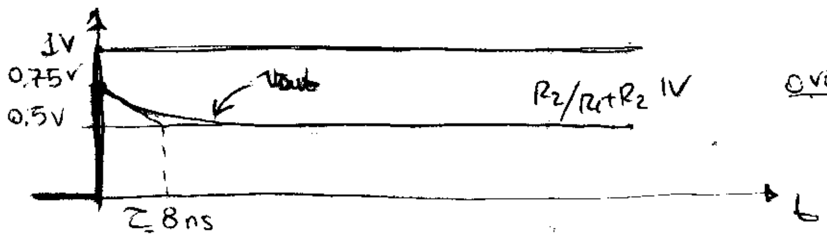
↳ capacitive divider.

$$V_{out}(0^+) = \frac{C_1}{C_1 + C_2} 1V = \frac{12pF}{16pF} 1V = 0.75V$$

$t \to \infty$; The capacitors are open circuits

↳ resistive divider

$$V_{out}(t \to \infty) = \frac{R_2}{R_1 + R_2} 1V = 0.5V$$



OVER COMPENSATED DIVIDER

In order to have a perfect step as output voltage ;

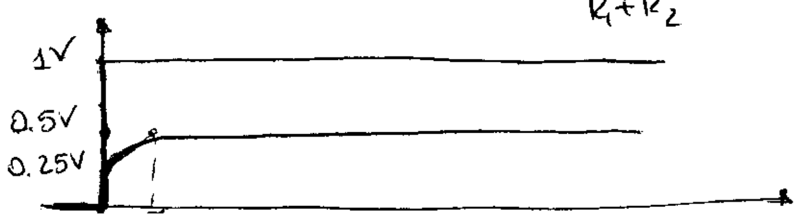
$$\frac{C_1}{C_1 + C_2} = \frac{R_2}{R_1 + R_2} \Rightarrow C_1R_1 + \cancel{C_1R_2} = R_2\cancel{C_1} + R_2C_2$$

COMPENSATED DIVIDER

If $R_1C_1 < R_2C_2$ (e.g. $C_1 = 4pF$; $C_2 = 12pF$; $R_1 = R_2 = 1k\Omega$)

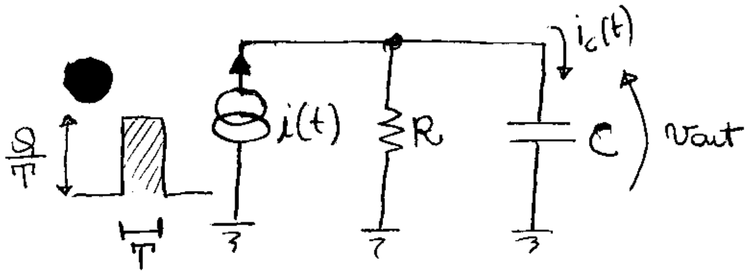
$$t = 0^+ \Rightarrow V_{out}(0^+) = \frac{C_1}{C_1 + C_2} 1V = \frac{4}{16} 1V = 0.25V$$

$$V_{out}(t \to \infty) = \frac{R_2}{R_1 + R_2} 1V = 0.5V$$



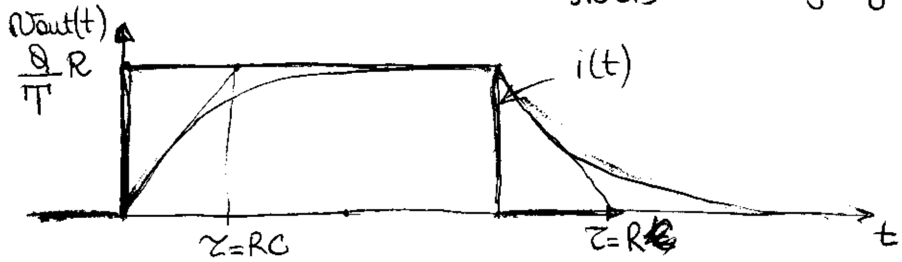
UNDER COMPENSATED DIVIDER

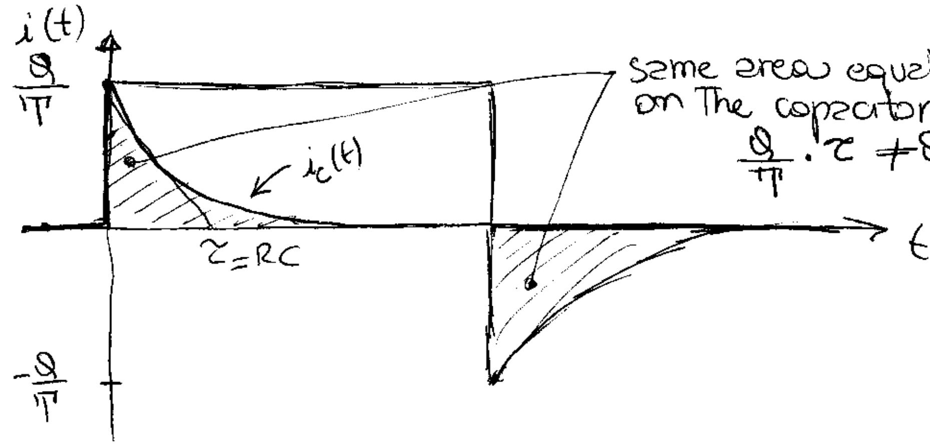
DELTA FUNCTION



$\tau = RC$

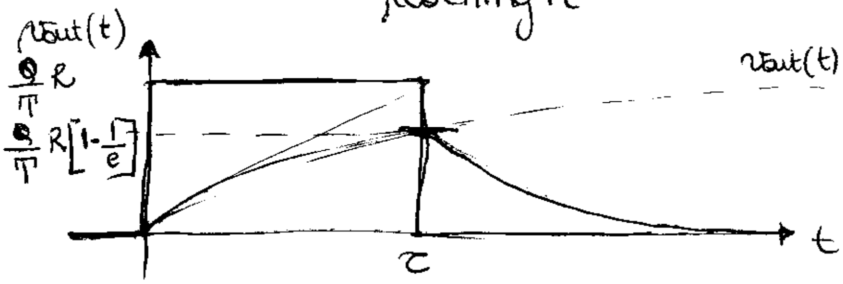
ⓐ $T \gg RC$ $\quad t = 0^+$ The capacitor cannot change its voltage drop
↳ The current flows in the capacitor that ~~becomes~~ starts charging



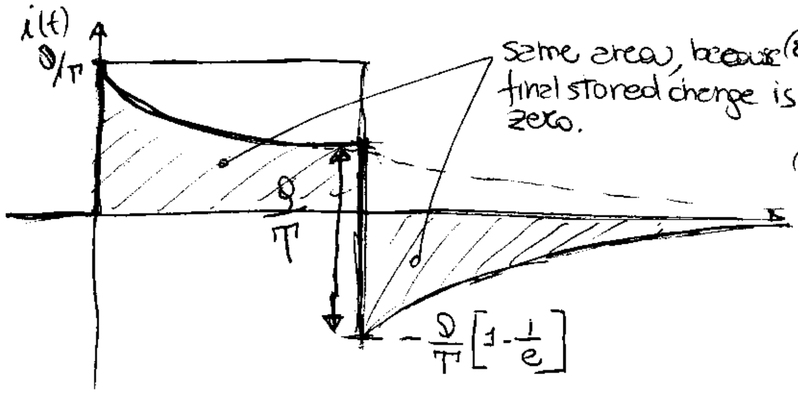


same area equal to the charge deposited on the capacitor plates
$\frac{Q}{T} \cdot \tau \neq Q$

ⓑ $T = RC$ ⇒ the capacitor cannot be fully charged to its maximum value, but it starts discharging before reaching it

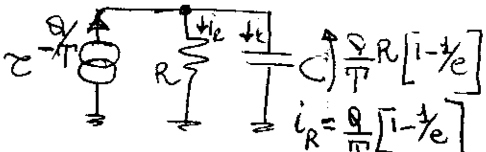


$v_{out}(t) = \frac{Q}{T}R\left(1 - e^{-t/\tau}\right)$



same area, because final stored charge is zero.

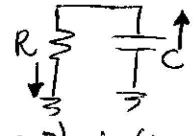
@ $t = \tau^-$



$i_R = \frac{Q}{T}\left[1 - \frac{1}{e}\right]$

$i_C = \frac{Q}{T}\frac{1}{e}$

@ $t = \tau^+$



$i_C(\tau^+) = -\frac{Q}{T}\left[1 - \frac{1}{e}\right]$

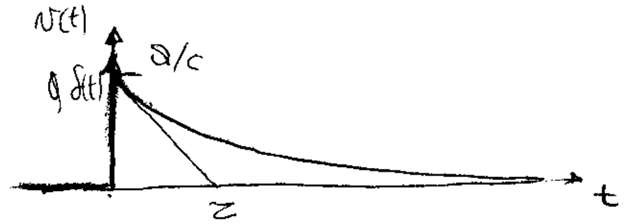
$i_R(t = \tau^-) = i_R(t = \tau^+)$

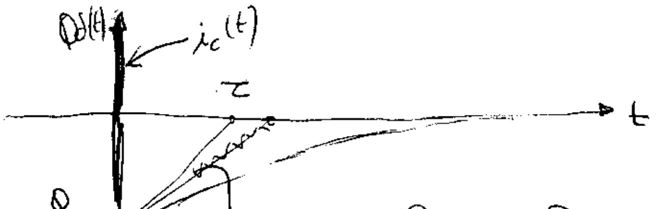
(c) $T \to 0$: we can introduce a novel function (generalized function) that is the delta pulse, i.e. the limit of the sequence of functions:

$$\delta(t) = \lim_{T \to 0} \frac{1}{T}\,\mathrm{rect}(T)$$

such that the area $\frac{Q}{T} \times T$ is always finite.

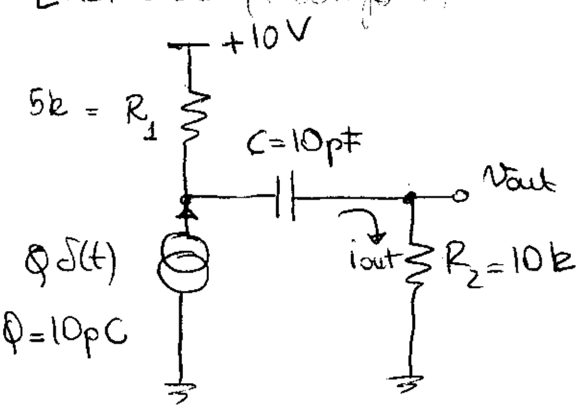
Since the pulse duration is much shorter than the circuit time constant, all the charge Q is deposited on the plates of the capacitor before a significant current can flow in the resistor.





area $= \frac{Q}{\tau} \cdot \tau = Q$ ok, capacitor has to be fully discharged

EXERCISE (mon pollo)



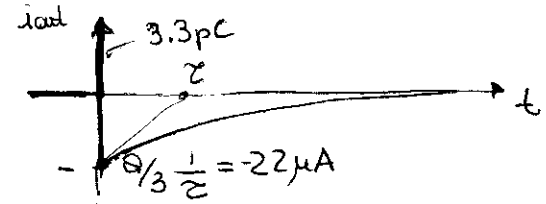
$\tau = C(R_1+R_2) = 150\,ns$

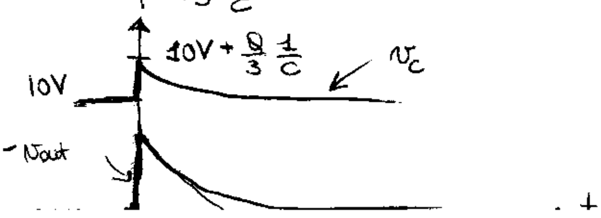
Draw the time diagram of Vout(t) and iout(t).

- $t<0$ — C is open circuit $\Rightarrow$ $V_{out}=0$, $i_{out}=0$ and the voltage drop across the capacitor is 10V
- $t=0$ — The capacitor has a negligible impedance (but can change its voltage drop thanks to the infinite current). Therefore we have a current divider

$$i_{out}(0^+) = Q\delta(t)\,\frac{R_1}{R_1+R_2} = 3.3pC\,\delta(t)$$

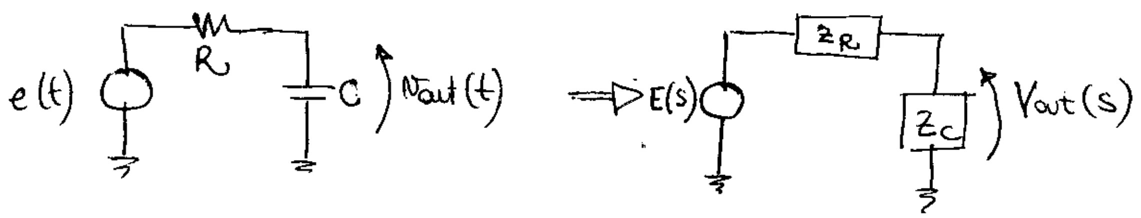
- $t>0$ — The voltage drop across the capacitor has to go back to the stationary condition





RC CIRCUIT IN THE FREQUENCY DOMAIN AND BODE DIAGRAMS

Let's consider again the RC circuit. By adopting the formalism of the Laplace transform we can look at the circuit in terms of the impedance of the bipoles:



$$V_{out}(s) = E(s)\,\frac{Z_C}{Z_R + Z_C} = E(s)\,\frac{\frac{1}{sC}}{R + \frac{1}{sC}} = E(s)\,\frac{1}{1+sCR}$$

$$\Downarrow$$

$$T(s) = \frac{V_{out}(s)}{E(s)} = \frac{1}{1+sCR}$$

TRANSFER FUNCTION
(That is the Laplace transform of the circuit response to a δ pulse)

The transfer function is generally a complex number that can be fully identified through its:

* AMPLITUDE or MAGNITUDE $|T(j\omega)|$: ratio between amplitudes of the output and the input sinusoidal signals $\forall\omega$
* PHASE $\arg[T(j\omega)]$: phase difference between the output and the input sinusoidal signals $\forall\omega$

where $T(j\omega)$ is the trace of $T(s)$ over the imaginary axis of the Gauss plane.

We can provide a graphical representation of the transfer function through the use of the Bode diagrams

* MAGNITUDE OF THE TRANSFER FUNCTION

It is a log-log diagram

- abscissa: frequency scale $f = \frac{\omega}{2\pi}$ expressed in $\log_{10}$ units
(The horizontal axis is $x = \log\frac{\omega}{\omega_{ref}}$; i.e. ω is normalised to a reference angular frequency, ω_{ref}, in order to obtain a dimensionless quantity and to fix the angular frequency of

The origin of the axis - Typically $\omega_{ref} = 1\,rad/s \Rightarrow x = \log\omega$)

- ordinate : we use a linear quantity : The DECIBEL, defined as

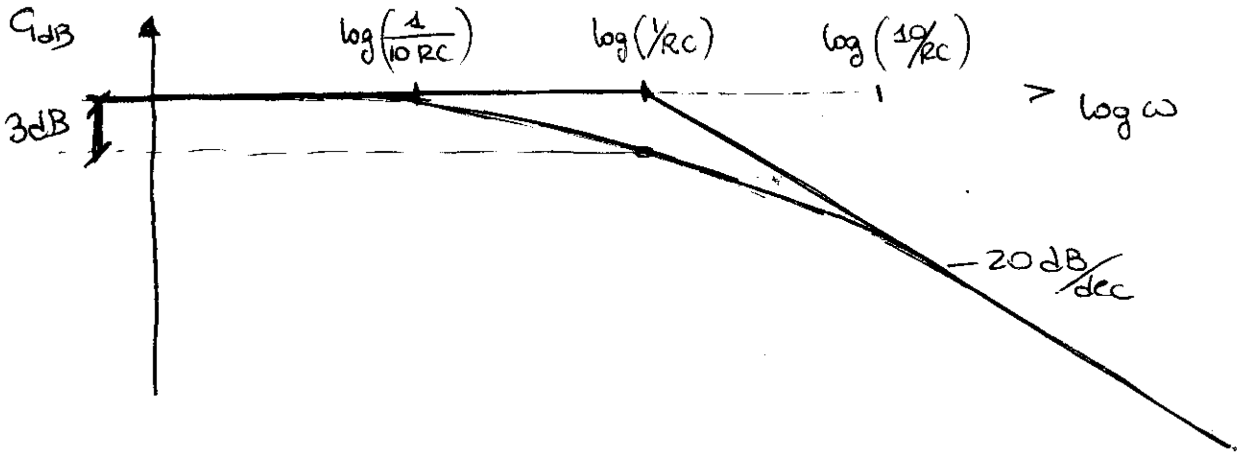
$$G = \left|T(j\omega)\right|_{dB} = 20\log_{10}\left|T(j\omega)\right|$$

⇓

$$G = 20\log_{10}\left|T(j\omega)\right| = 20\log_{10}\left|\frac{1}{1+j\omega RC}\right| = 20\log_{10}\frac{1}{\sqrt{1+\omega^2R^2C^2}}$$

Let's study the asymptotic behavior of this function

- $\omega \ll \frac{1}{RC}$ (i.e. $R \ll \frac{1}{\omega C}$) $\Rightarrow G = 0\,dB$
- $\omega \gg \frac{1}{RC}$ (i.e. $R \gg \frac{1}{\omega C}$) $\Rightarrow G \simeq -20\log_{10}\omega RC$
  ↳ linear behaviour with slope of $-20\,dB$ every decade



The maximum distance between the asymptotic behavior and the real behaviour occurs at $\omega = \frac{1}{RC}$ where:

$$G\left(\omega = \frac{1}{RC}\right) = 20\log_{10}\frac{1}{\sqrt{2}} = -3\,dB$$

The two diagrams overlap ~~starting~~ up to one decade before $1/RC$ (the pole of the transfer function) and starting from one decade after $1/RC$

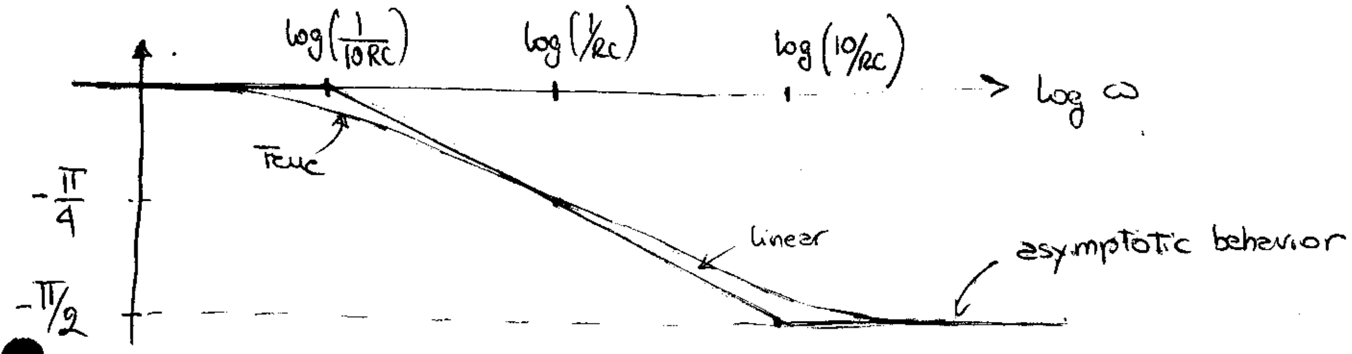
⇓ LOW FREQUENCY ($f \ll \frac{1}{2\pi RC}$) : no attenuation, the capacitor has a reactance much higher than the resistance → no effect

HIGH FREQUENCIES ($f \gg \frac{1}{2\pi RC}$) : The output signal is attenuated w.r.t input signal ⇒ LOW PASS FILTER

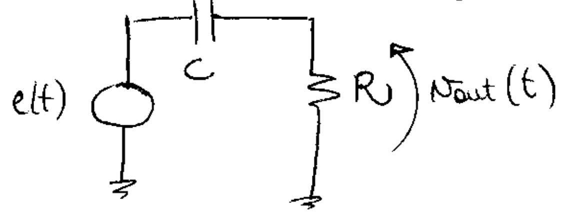
* PHASE :

$$\arg\left[T(j\omega)\right] = -\,\text{artg}(\omega RC)$$

- $\omega RC \gg 1 \rightarrow \varphi = -\frac{\pi}{2}$
- $\omega RC = 1 \rightarrow \varphi = -\frac{\pi}{4}$
- $\omega RC \ll 1 \rightarrow \varphi = 0$



With a similar analysis we can conclude That The CR circuit



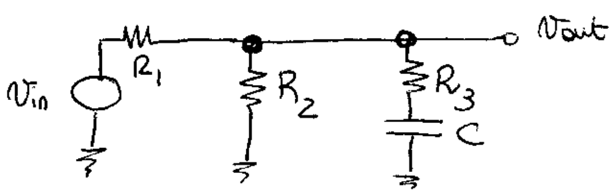
Whose Transfer function is

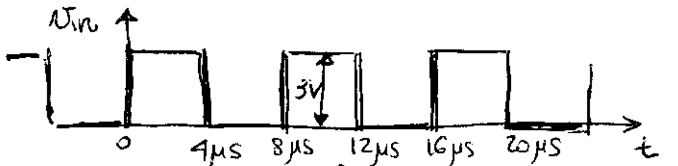
$$T(s) = \frac{R}{R+\frac{1}{sC}} = \frac{sCR}{1+sCR} \Rightarrow T(j\omega) = \frac{\omega CR}{1+\omega CR}$$

is an HIGH PASS FILTER, since at frequencies lower Than The pole The reactance of The capacitor is larger Than The resistance and Therefore The amplitude of the output sinusoidal signal is greatly reduced with respect To The input one, while at frequencies much higher Than The one of The pole The capacitor reactance is definitely much lower Than The resistance $\Rightarrow$ The Transfer is nearly close to unity.

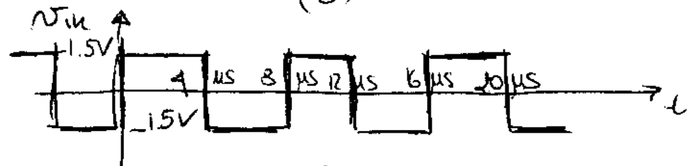
EXERCISE (from ...)

Let's consider the following circuit:





(a)



(b)

$R_1 = 2k\Omega$ $\quad R_2 = 6k\Omega$
$R_3 = 3k\Omega$ $\quad C = 50pF$

1. Draw the time diagram of the output voltage, v_{out}, quoting all the relevant points, when the input signal is the one shown in (a)

2. Draw the time diagram of the output voltage, v_{out} quoting all the relevant points, when the input signal is the one shown in (b)

It is a single time-constant circuit.
First of all, let's compute the circuit time constant:

$$\tau = C\left(R_3 + R_2 \| R_1\right) = 225\ ns$$

Therefore the output waveform has the time needed to reach the "final" voltage within every half period.

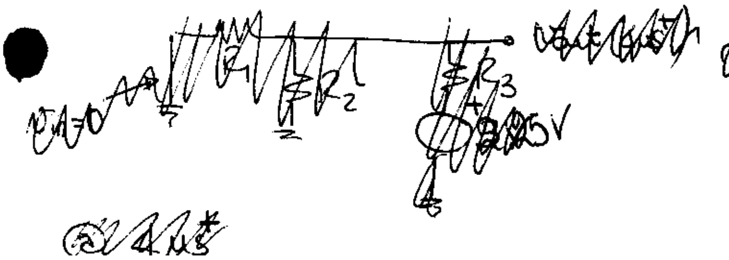
To determine the complete behaviour of the output voltage, let's compute the output voltage at the transition and its final value.

FINAL
$\begin{cases} * \text{ when } v_{in} = 3V \Rightarrow \text{final value } v_{out} = \dfrac{R_2}{R_1+R_2} v_{in,max} = \dfrac{6k\Omega}{8k\Omega} 3V = 2.25V \\ * \text{ when } v_{in} = 0V \Rightarrow \text{final value } v_{out} = \dfrac{R_2}{R_1+R_2} v_{in,min} = 0V \end{cases}$

Before the transition at $t=0^+$, $v_{out}(0^-) = 0V$ and $\Delta v_c(0^-) = 0V$ hence due to the constraint imposed by the capacitor $(\Delta v_c(0^+) = \Delta v_c(0^-))$

$$\rightarrow v_{out}(t=0^+) = \frac{R_3 \| R_2}{R_1 + R_3 \| R_2} v_{in,max} = \frac{2k\Omega}{4k\Omega} 3V = 1.5V$$

The same procedure applies to the transition at $t = 4\mu s$; before this transition $v_{out}(4\mu s^-) = 2.25V$ therefore $\Delta v_c(4\mu s^-) = 2.25V$
~~Due to the constraint imposed by the capacitor, at $t = 4\mu s^+$ the circuit becomes:~~



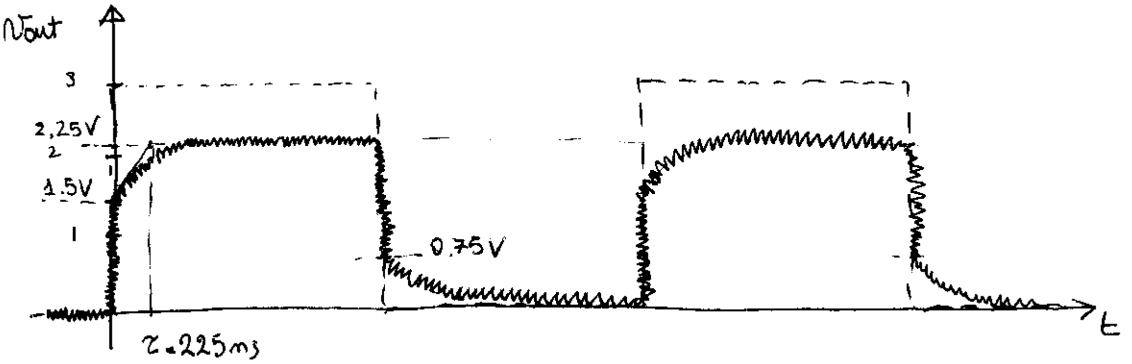
~~$v_{out}(4\mu s^+) = \dfrac{R_1 \| R_2}{R_3 + R_1 \| R_2} 2.25V$~~

~~$= \dfrac{3/2\,k\Omega}{(3+3/2)k\Omega} 2.25V = \dfrac{1}{3} 2.25V$~~ $= 0.75V$

~~@ $4\mu s^+$~~

We can look at the input signal as showing a negative transition of 3V, therefore from the value of 2,25V we will have a step down of $\frac{R_3 \| R_2}{R_1 + R_3 \| R_2} * (-3V) = -1.5V$

The value of the output voltage at $t = 4\mu s^+$ will be $2{,}25V - 1.5V = 0.75V$

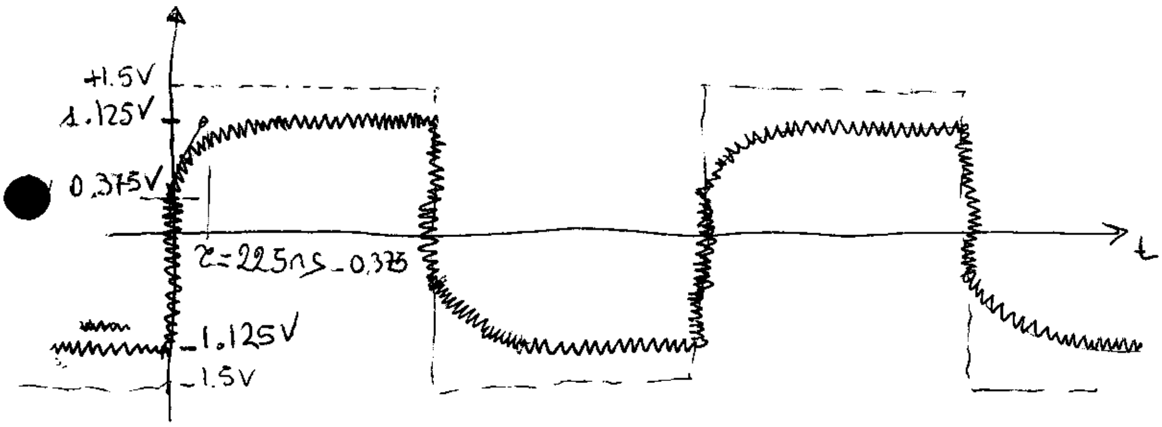


2. We can look to the square wave in (b) as the square wave shown in (a) plus a constant voltage of $-1.5V$. Since the circuit is linear we can apply the superposition theorem. We already know the output voltage when the square wave in (a) is applied. Therefore we have only to compute the contribution to the output of a DC voltage source of $-1.5V$. The capacitor will be, obviously, an open circuit.

$$v_{out}\Big|_{-1.5V} = -1.5V \cdot \frac{R_2}{R_1+R_2} = -1.125V$$

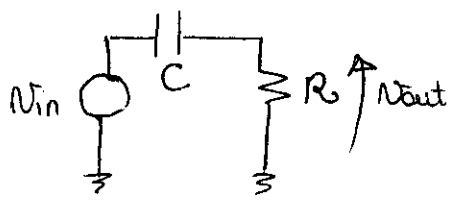
Therefore the output voltage, previously calculated, has to be shifted of $-1.125V$.

The resulting time diagram will be:

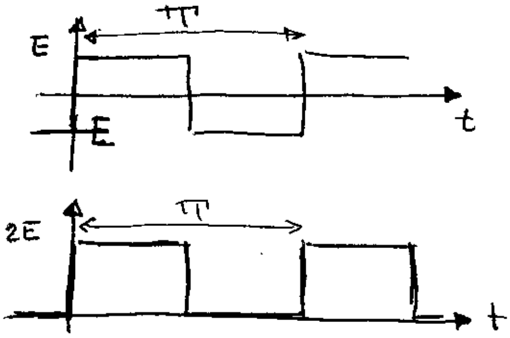


EXERCISE (mom 10th)

Let's consider the following circuit:



$R = 2k\Omega$, $C = 100pF$



(a) $T = 10\mu s$

$E = 1V$

(b) $T = 10\mu s$

1. Draw the time diagram of the output voltage for v_{in} shown in (a)
2. Draw the time diagram of the output voltage v_{out} for v_{in} shown in (b)
3. Draw the time diagram of the output voltage v_{out}, for the input signal shown in (a) when the period of the square wave is 400ns. (Assume the circuit reached the steady state)

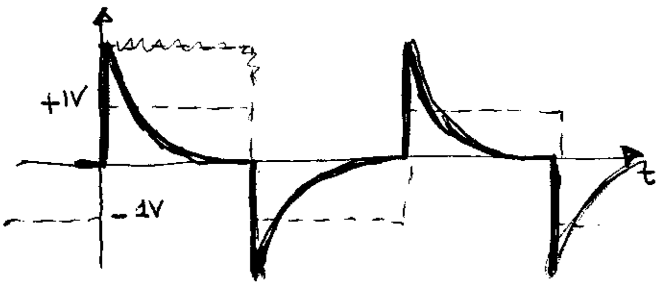
1. $\tau = RC = 200\,ns$ → The circuit reaches the steady state in each half period.

$t = 0^-$: $v_{out} = 0 \rightarrow \Delta V_C(0^-) = -E$

$\Downarrow$ @ $t = 0^+$ $\Delta V_C(0^+) = \Delta V_C(0^-) = -E \Rightarrow v_{out} = v_{in} - \Delta V_C = E + E = 2E$

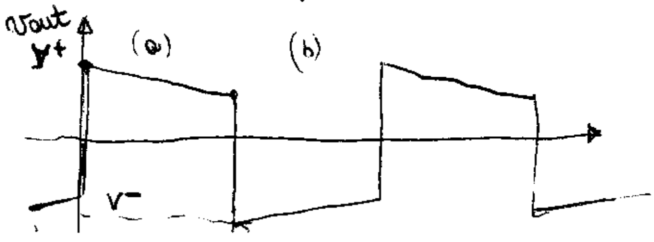
$t = 0^-$: $v_{out} = 0 \rightarrow \Delta V_C(0^-) = +E$

$\Downarrow$ @ $t = 0^+$ $\Delta V_C(0^+) = \Delta V_C(0^-) = +E \Rightarrow v_{out} = v_{in} - \Delta V_C = -E - E = -2E$



2. Again we can look at the input signal as the one shown in (a) plus a DC constant voltage equal to the mean value of the signal in (b) (i.e. 1V)
The mean value is a DC voltage ⇒ it gives no contribution at the output of a CR network ⇒ the time diagram will be the same as in 1.

3. $\frac{T}{2} = \tau \Rightarrow$ The circuit do not saturate to the final value in each half period.

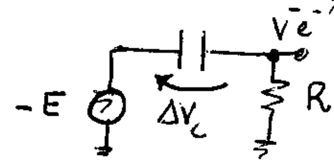


The output will resemble more a square wave.

$V^+ > 0$
$V^- < 0$

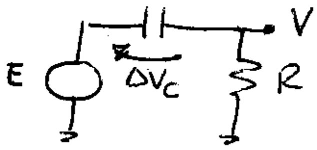
We have to compute the values V^+ and V^-. We can write the relationship of the voltage signal during half period (a) and (b) at the transiti

@ $t = 0^+$



$\Delta V_C = -E - V^- e^{-T/2/\tau}$

@ $t = 0^+$

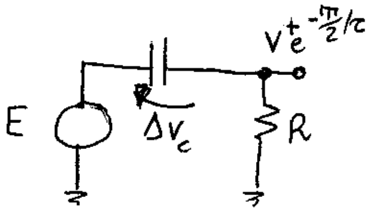


but $\Delta V_c(0^+) = \Delta V_c(0^-)$

$\Delta V_c(0^+) = E - V^+$

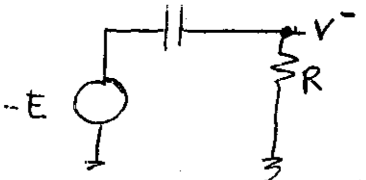
$\hookrightarrow +E - V^+ = -E - V^- e^{-1}$

@ $t = 0^-$



$\Delta V_c = E - V^+ e^{-T/2/\tau}$

@ $t = 0^+$



$\Delta V_c(0^+) = -E - V^-$

but $\Delta V_c(0^+) = \Delta V_c(0^-)$

$\hookrightarrow -E - V^- = E - V^+ e^{-1}$

$$\begin{cases} E - V^+ = -E - V^- e^{-1} \\ -E - V^- = E - V^+ e^{-1} \end{cases}$$

two equations in two unknown V^+ and V^-

$\Downarrow$

$V^+ = E + E + V^- e^{-1} = 2E + V^- e^{-1}$ (from 1st equation)

Inserting V^+ in 2nd equation:

$-E - V^- = E - (2E + V^- e^{-1}) e^{-1}$

$-V^-(1 - e^{-2}) = 2E - 2Ee^{-1}$

$$V^- = \frac{2E(e^{-1} - 1)}{1 - e^{-2}} = \frac{-2V \times 0.632}{0.865} = -1.46$$

$\hookrightarrow V^+ = 2V + (-1.46V)e^{-1} = 1.46$ (obviously: duty cycle 50% and zero average value)