Politecnico di Milano

Microcontrollori 2/3

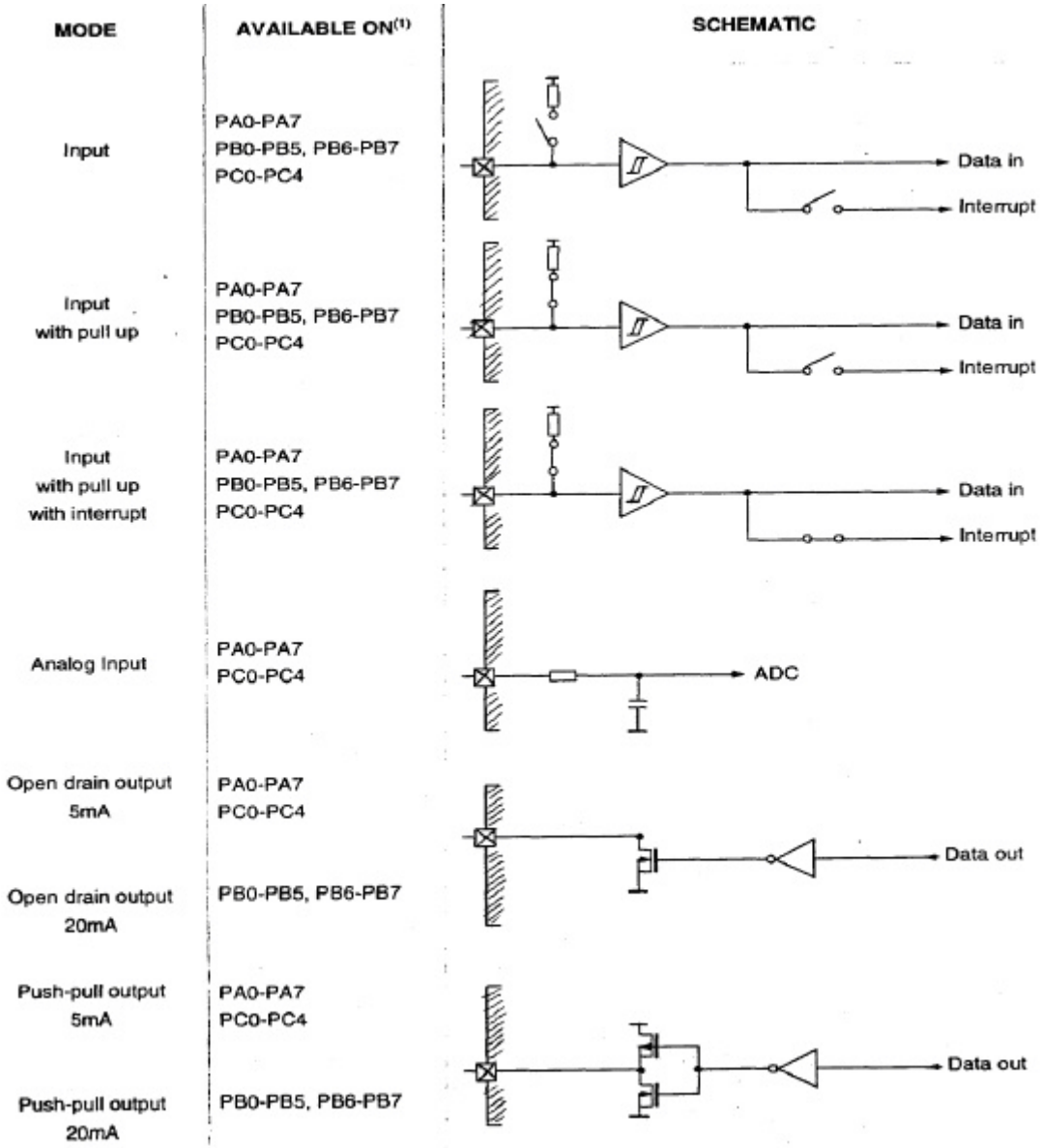
ing. Enrico Migliore

Fondamenti di Elettronica

Porte di I/O

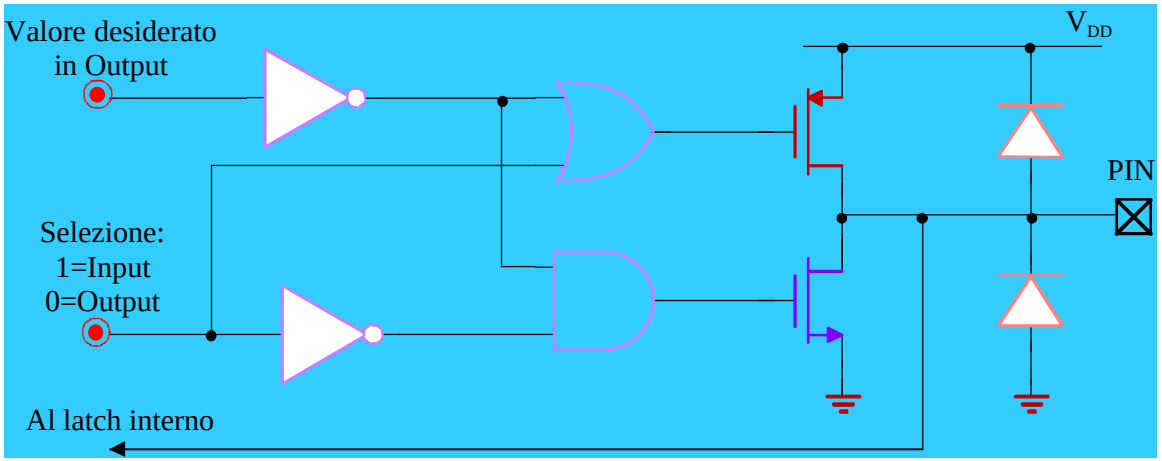
Tipologie:

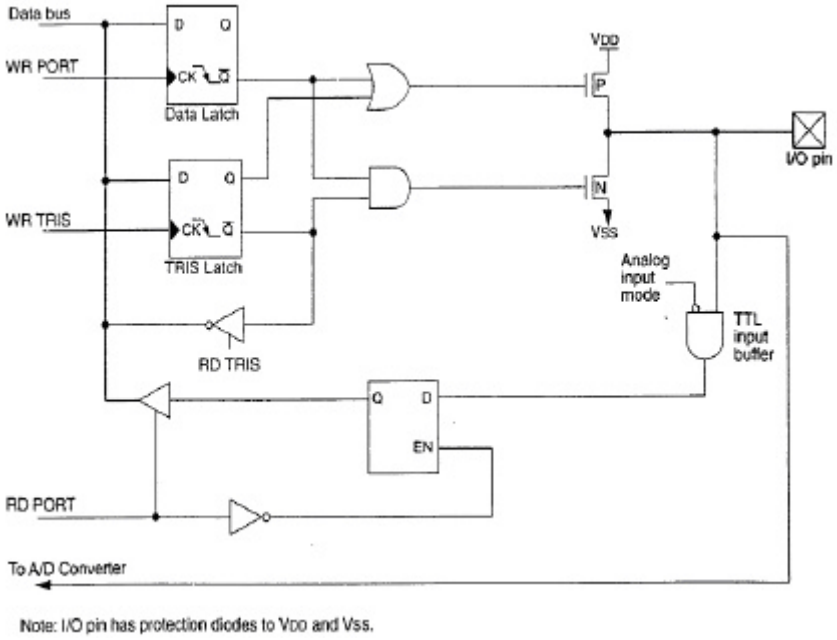
- Input digitale
  - •ingresso CMOS normale
  - •o a trigger di Schmidt
  - •a volte con pull-up
- Input con Interrupt
  - •abilitato a generare
  - •un interrupt nel µC
- Input analogico
  - •per inviare segnali
  - •analogici all'ADC del µC
- Output digitale
  - •normalmente livelli CMOS
  - •a volte open-drain
  - •può avere pull-up interno
  - •può essere tri-state



Porte di I/O

Inizializzazione interna dei pin di I/O:





Note: I/O pin has protection diodes to VDD and Vss.

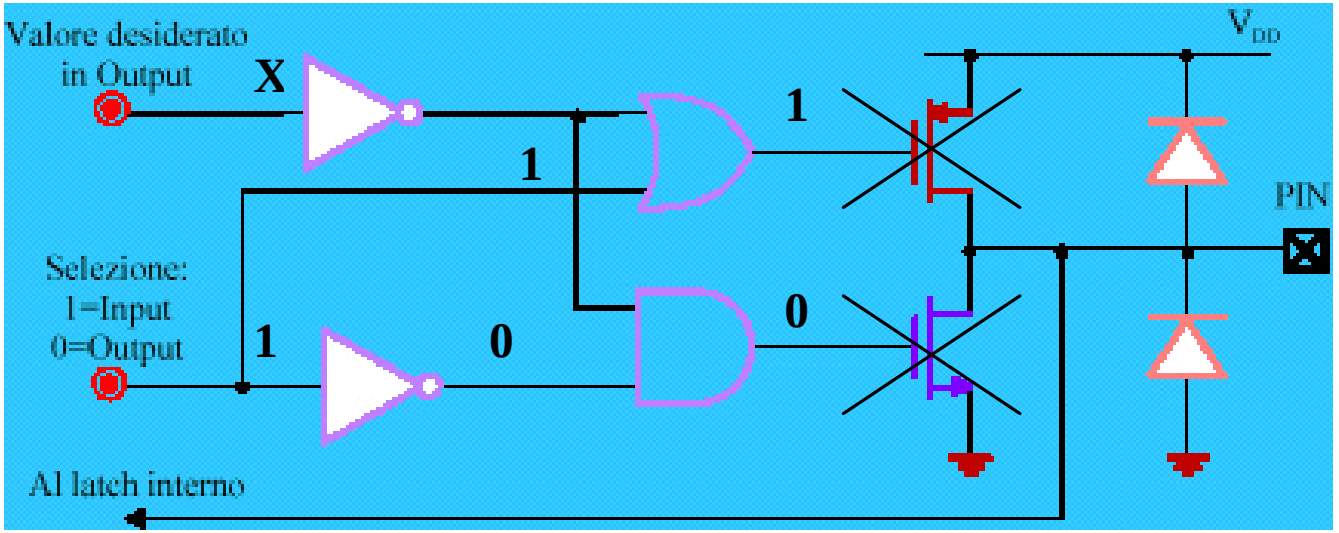
PIC16C74A:

EXAMPLE INITIALIZING PORTA:

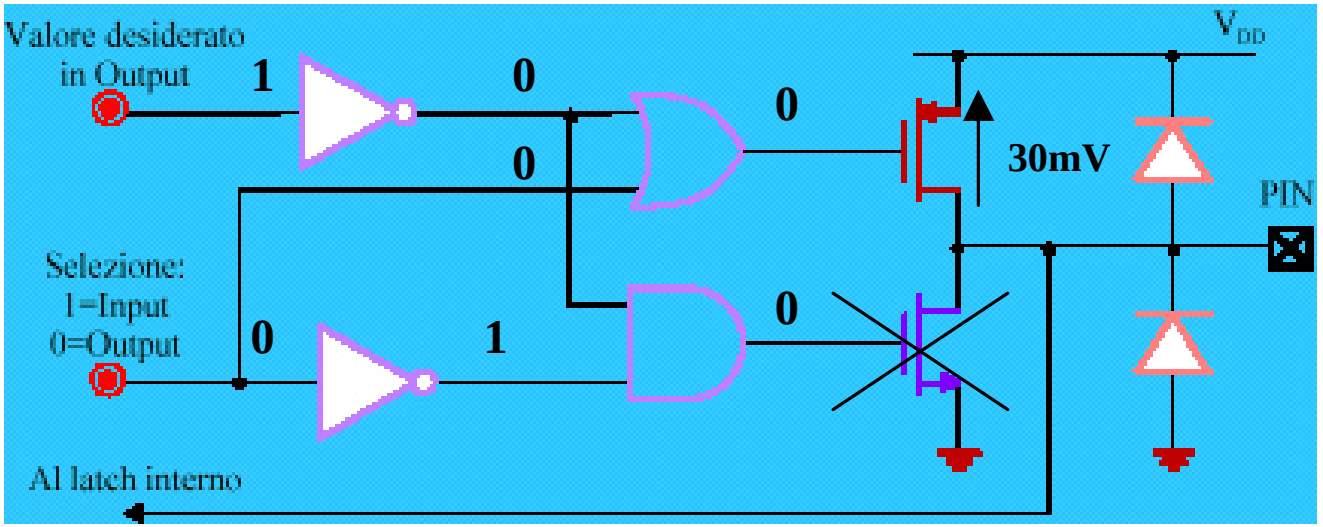
```
CLRF PORTA          ;Initialize PORTA by clearing output latches
BSF STATUS, RPO     ;Select Bank 1
MOVLW 0xCF          ;initialize data direction 11001111
MOVWF TRISA         ;Set RA<3:0> as inputs
                    ;RA<5:4> as outputs
                    ;TRISA<7:6> always read as '0'
```

Porte di I/O

PORTA CONFIGURATA IN INGRESSO



PORTA CONFIGURATA IN USCITA



Interrupt

Idea base: la CPU sta eseguendo il programma principale. Si verifica un evento (es. un pin d'ingresso cambia stato) che necessita in tempi brevi di essere riconosciuto dalla CPU….

Modalità di gestione:

- vettore di interrupt — ogni periferica chiamante ha la sua routine di gestione
- polling — c'è un'unica routine; il firmware dovrà individuare la periferica chiamante

Stack:

- salvare il ProgramCounter — per sapere da dove continuare, una volta gestita la routine di interrupt
- salvare i registri importanti — per evitare di modificare dati importanti

```
MOVWF   W_TEMP          ;Copy W to TEMP register, could be bank one or zero
SWAPF   STATUS,W        ;Swap status to be saved into W
BCF     STATUS,RP0      ;Change to bank zero, regardless of current bank
MOVWF   STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF   STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF   STATUS          ;Move W into STATUS register
SWAPF   W_TEMP,F        ;Swap W_TEMP
SWAPF   W_TEMP,W        ;Swap W_TEMP into W
```

Interrupt

Utilità:

- gestire eventi imprevedibili — allarme, finecorsa, pulsante…
- evitare cicli di attesa — non si continua a monitorare l'evento, poiché sarà lui a chiamare
- eseguire prontamente routine — per ogni chiamante si eseguiranno operazioni distinte

Modalità di gestione:

- vettore di interrupt — ogni periferica chiamante ha la sua routine di gestione
- polling — c'è un'unica routine; il firmware dovrà individuare la periferica chiamante

Stack:

- salvare il ProgramCounter — per sapere da dove continuare, una volta gestita la routine di interrupt
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```
MOVWF   W_TEMP          ;Copy W to TEMP register, could be bank one or zero
SWAPF   STATUS,W        ;Swap status to be saved into W
BCF     STATUS,RP0      ;Change to bank zero, regardless of current bank
MOVWF   STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF   STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF   STATUS          ;Move W into STATUS register
SWAPF   W_TEMP,F        ;Swap W_TEMP
SWAPF   W_TEMP,W        ;Swap W_TEMP into W
```

Interrupt

Gestione:

- impostando dei registri dedicati — abilitazione/disabilitazione dell'interrupt, flag dell'avvenuta chiamata…
- firmware della routine — …

INTCON REGISTER FOR PIC16C72/73/73A/74/74A (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note 1: For the PIC16C73 and PIC16C74, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may be unintentionally re-enabled by the `RETFIE` instruction in the user's Interrupt Service Routine. Refer to Section 14.5 for a detailed description.

PIE1 REGISTER PIC16C73/73A/74/74A (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIE**(1)**:** Parallel Slave Port Read/Write Interrupt Enable bit
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6: **ADIE**: A/D Converter Interrupt Enable bit
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5: **RCIE**: USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4: **TXIE**: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3: **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE**: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE**: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

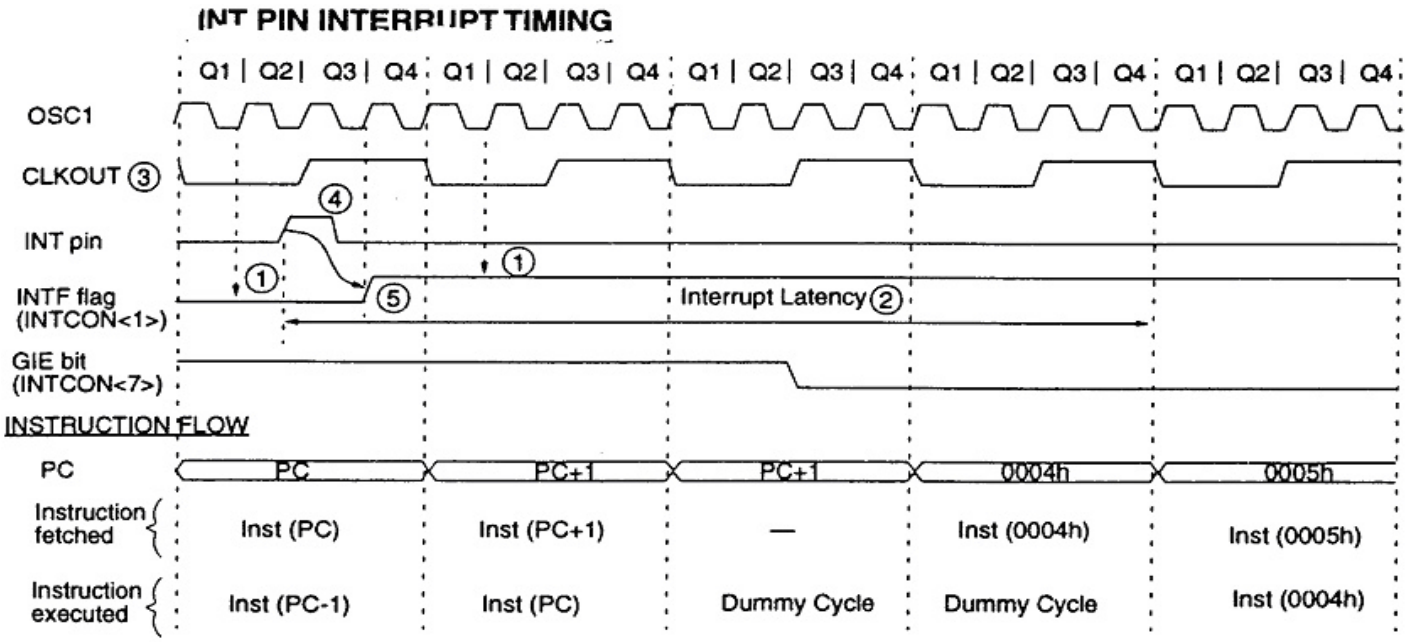
bit 0: **TMR1IE**: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Note 1: PIC16C73 and PIC16C73A devices do not have a Parallel Slave Port implemented, this bit location is reserved on these two devices, always maintain this bit clear.

Interrupt

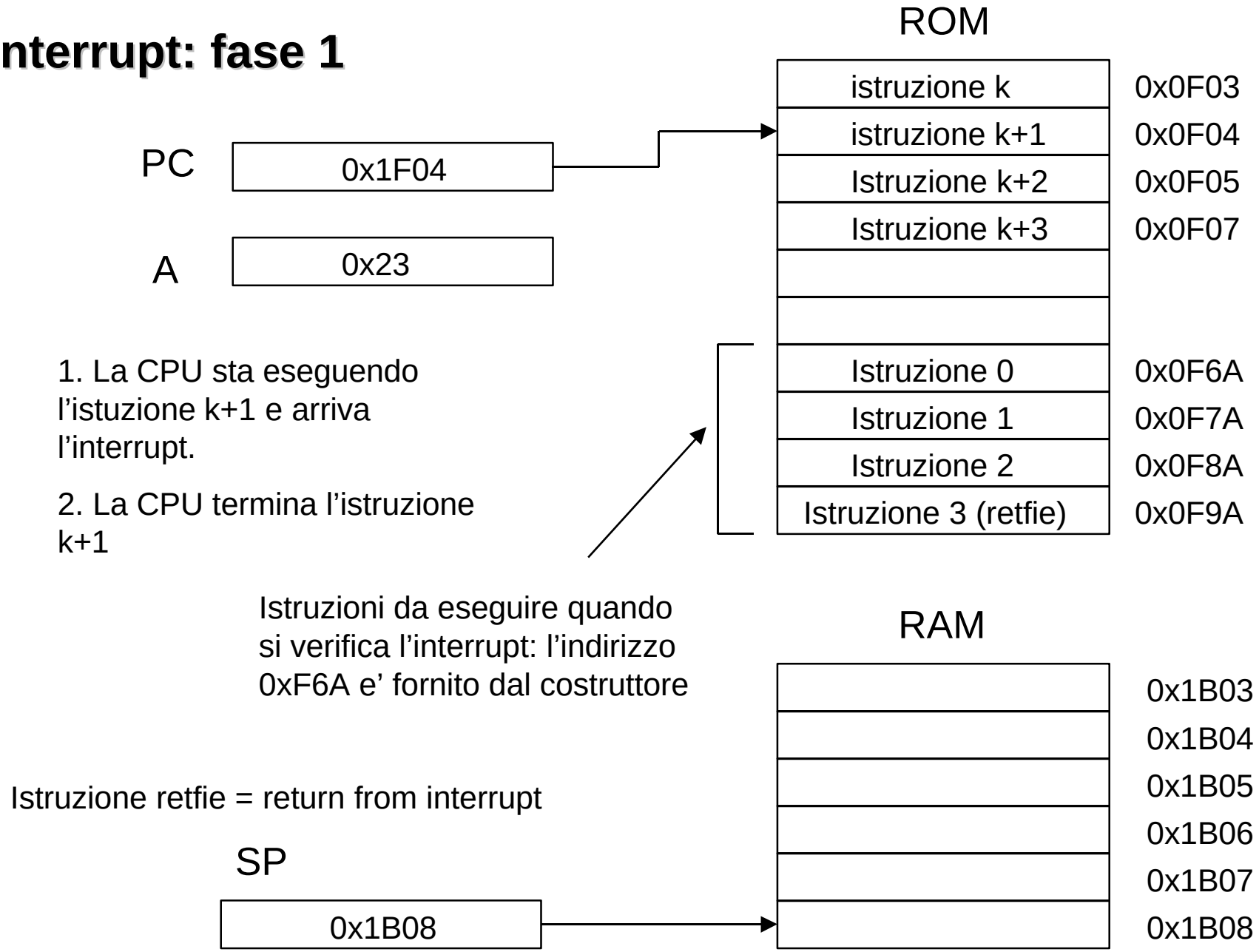
Latenza:

- esecuzione non immediata della routine di interrupt
- temporizzazione

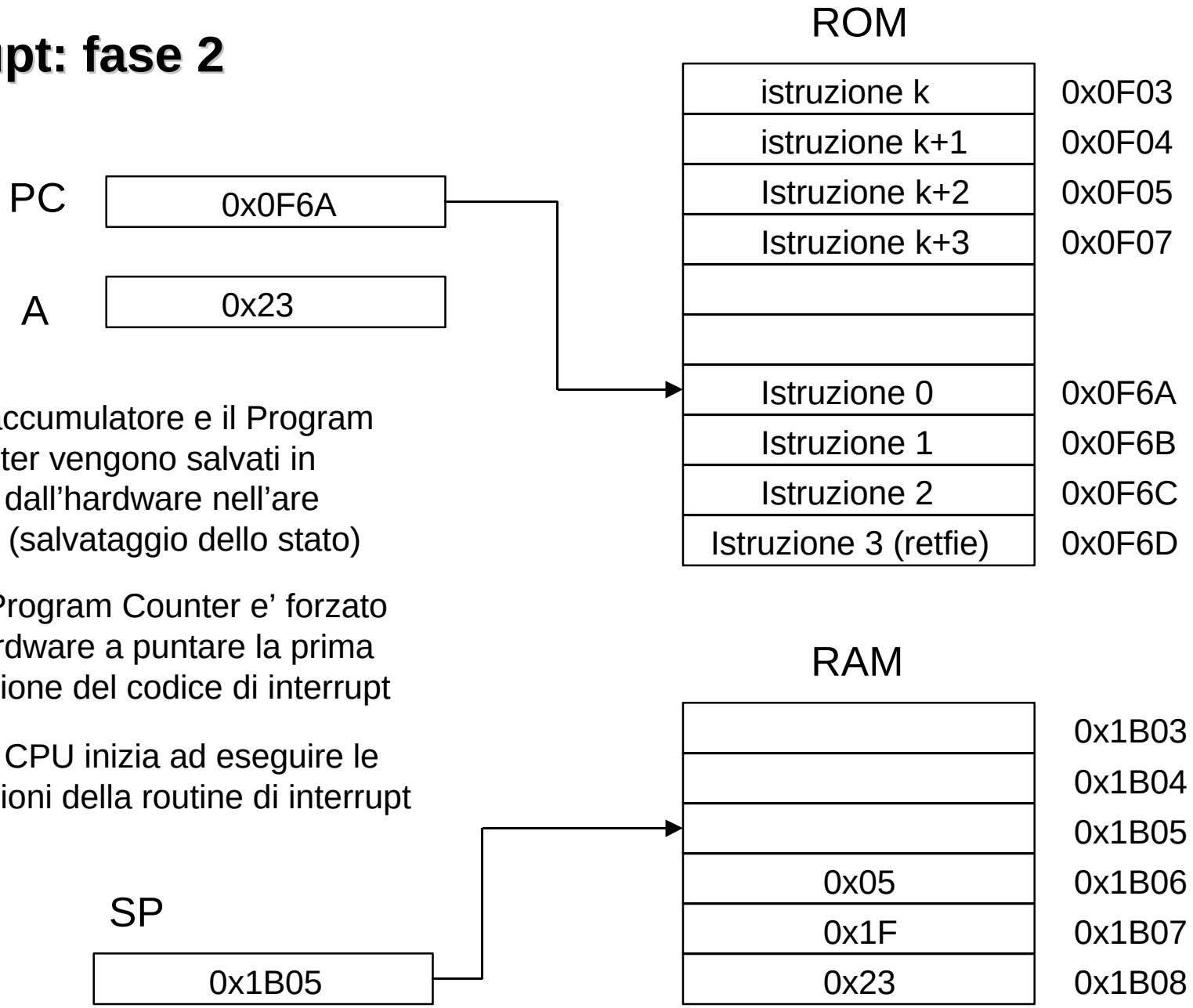


Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

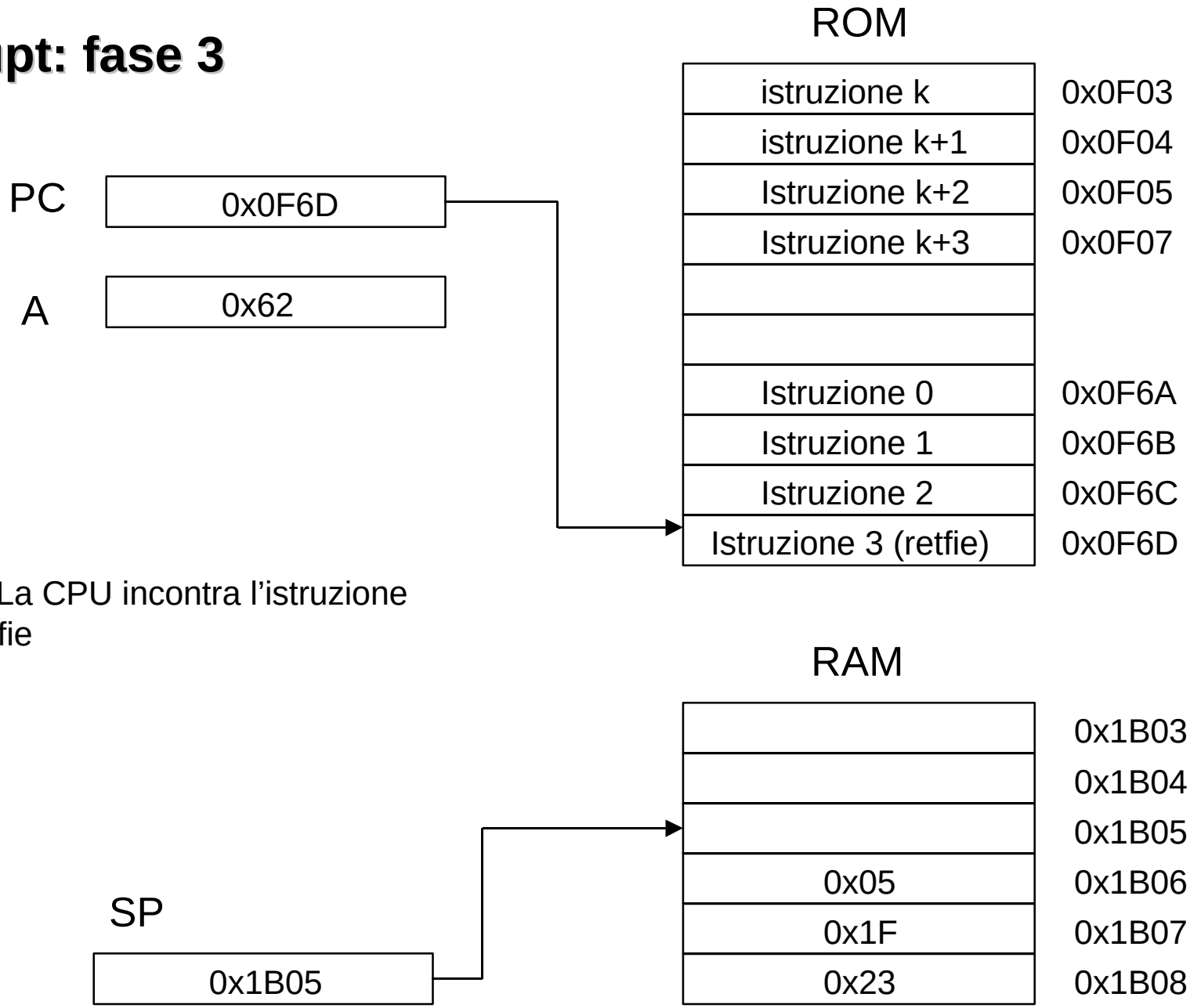
Interrupt: fase 1



Interrupt: fase 2

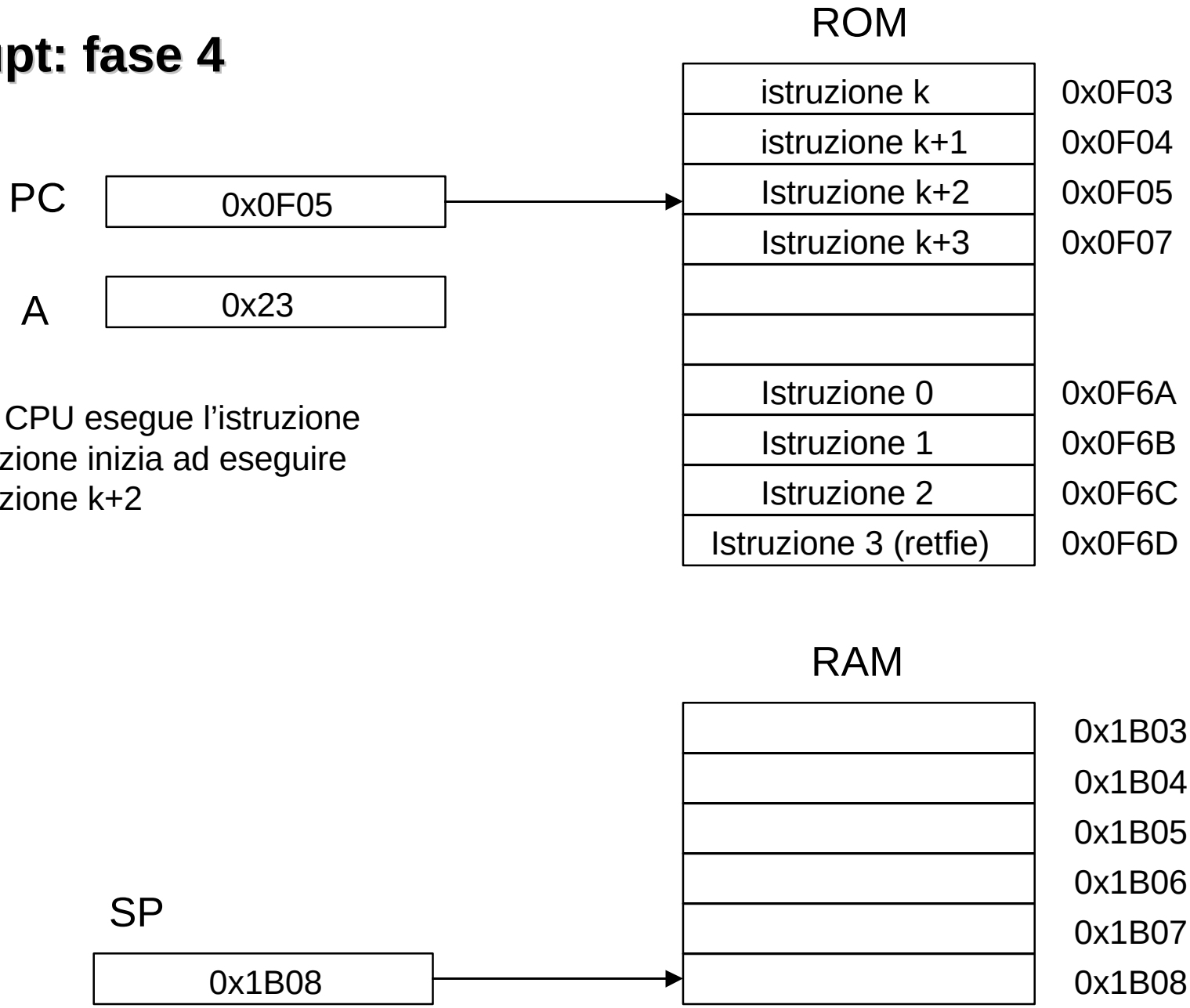


Interrupt: fase 3



1. La CPU incontra l'istruzione retfie

Interrupt: fase 4



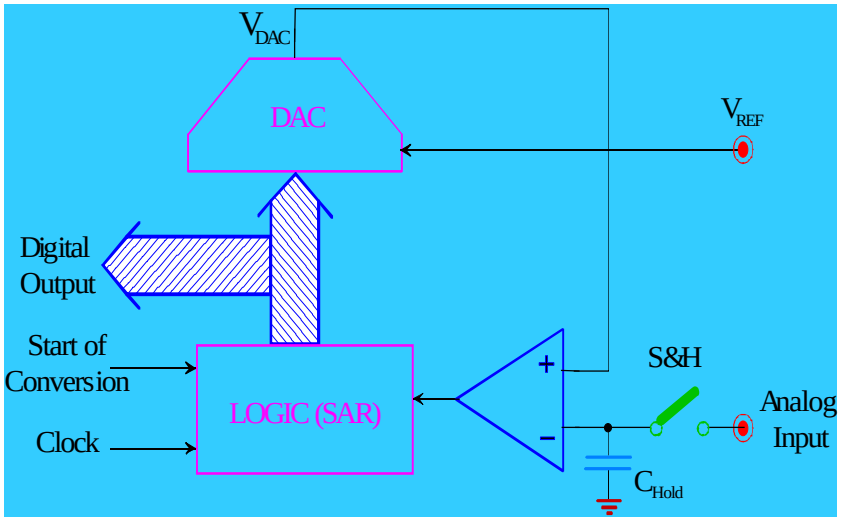
ADC

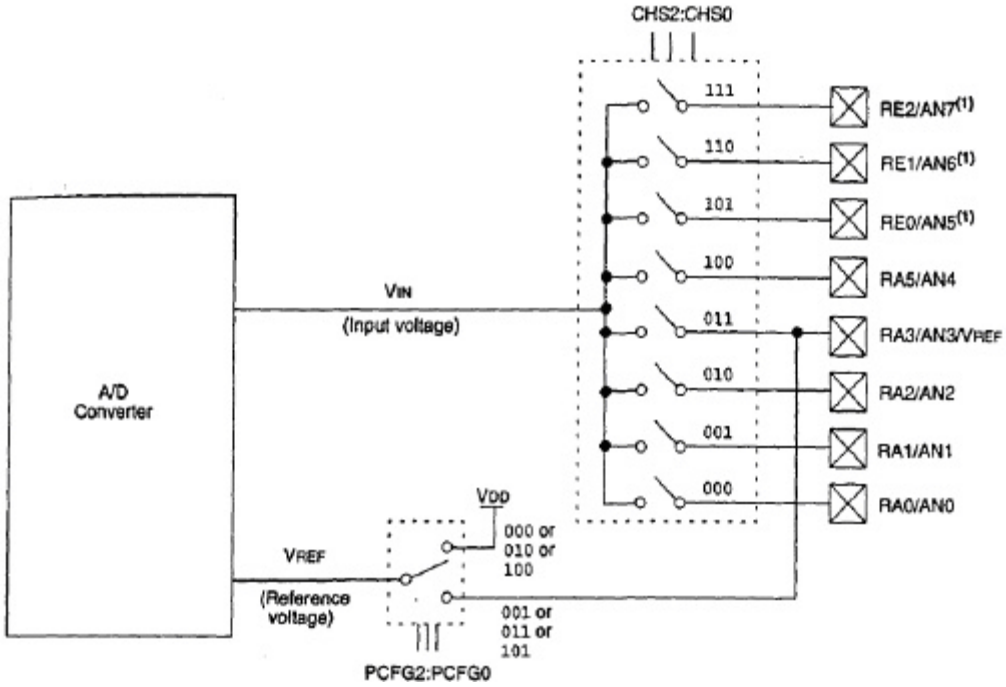
Convertitore Analogico/Digitale:

- multiplexer analogico a più ingressi
- campionatore S&H
- ADC (SuccessiveApproximationRegister)

Risoluzione:

- numero di bit n
- FullScaleRange FSR = V_{ref}
- LeastSignificantBit LSB = FSR / 2^n





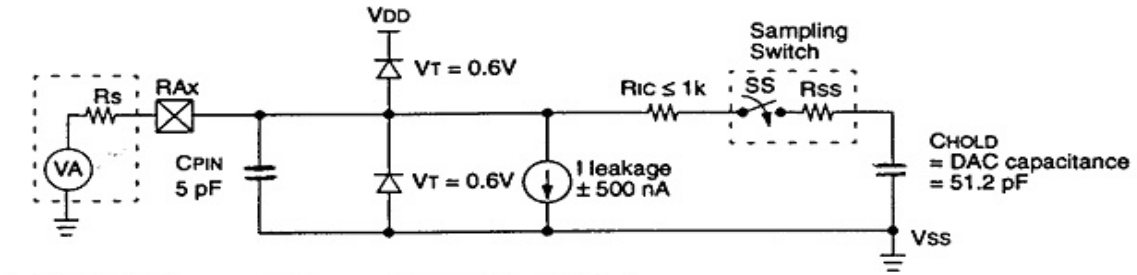
ADC

Errori:

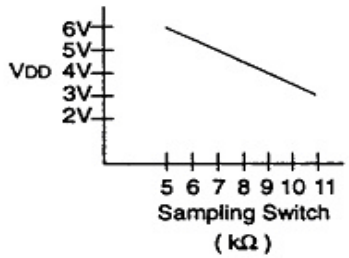
- statici — correnti di leakage, resitenze parassite — $R_S < ½LSB / I_{leakage} = 10k\Omega$
- dinamici — carica esponenziale del condensatore del S&H — $V_{ref} - ½LSB = (1- e^{-t/\tau})\cdot V_{ref}$

Tempistiche:

- di acquisizione — carica esponenziale di C_{HOLD} — $T_a = -C_{HOLD}\left(R_S + R_{IC} + R_{SS}\right)\cdot \ln \frac{½\,LSB}{V_{ref}} = 5.7\mu s$
- di conversione — durata della conversione nell'ADC — $T_{conv} = 9.5\cdot T_{AD}$



Legend
CPIN = input capacitance
VT = threshold voltage
I leakage = leakage current at the pin due to various junctions
RIC = interconnect resistance
SS = sampling switch
CHOLD = sample/hold capacitance (from DAC)



PIC16C74A

ADC

Configurazione:

- tramite registri dedicati

```
BSF STATUS, RPO      ; Select Page 1
CLRF ADCON1          ; Configure A/D inputs
BSF PIE1,ADIE        ; Enable A/D interrupts
BCF STATUS,  RPO     ; Select Page 0
MOVLW 0XC1           ; A/D is on , Ch0 is selected
MOVWF ADCON0         ;
BCF PIR1, ADIF       ; Clear A/D interrupt flag bit
BSF INTCON, PEIE     ; Enable peripheral interrupts
BSF INTCON, GIE      ; Enable all interrupts
     :
BSF ADCON, GO        ; Start A/D Conversion
     :
```

ADCON0 REGISTER, PIC16C72/73/73A/74/74A (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from an RC oscillation)

bit 5-3: **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)(1)
110 = channel 6, (RE1/AN6)(1)
111 = channel 7, (RE2/AN7)(1)

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Unimplemented:** Read as '0'

bit 0: **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

ADCON1 REGISTER, PIC16C72/73/73A/74/74A (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-3: **Unimplemented:** Read as '0'

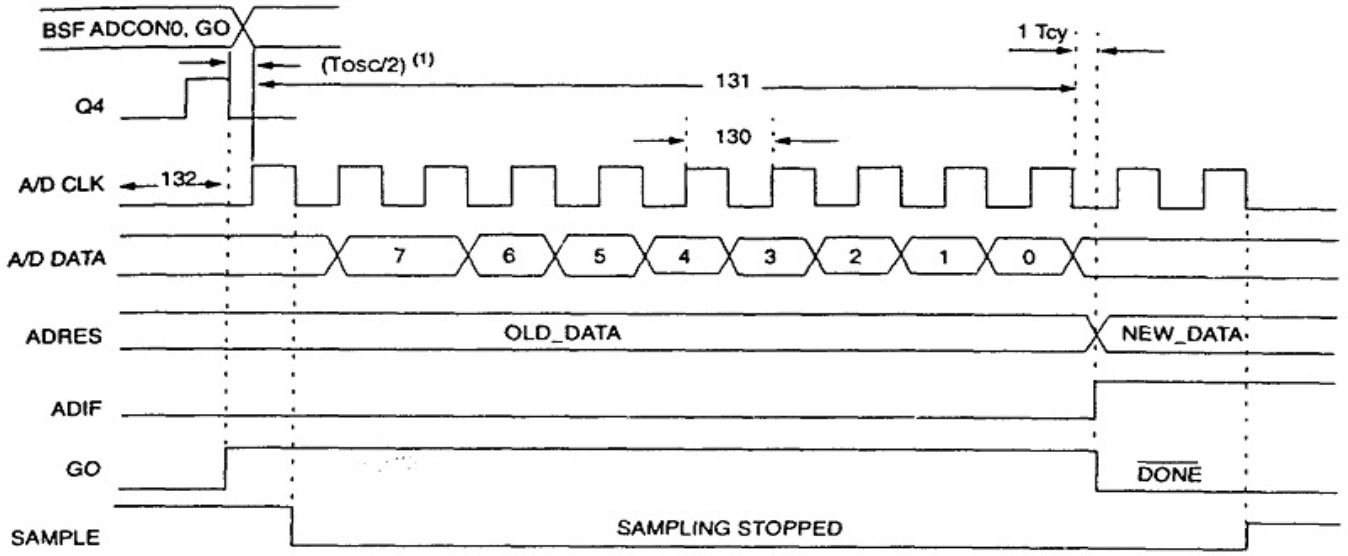
bit 2-0: **PCFG2:PCFG0:** A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	RE0(1)	RE1(1)	RE2(1)	VREF
000	A	A	A	A	A	A	A	A	VDD
001	A	A	A	A	VREF	A	A	A	RA3
010	A	A	A	A	A	D	D	D	VDD
011	A	A	A	A	VREF	D	D	D	RA3
100	A	A	D	D	A	D	D	D	VDD
101	A	A	D	D	VREF	D	D	D	RA3
11x	D	D	D	D	D	D	D	D	—

A = Analog input
D = Digital I/O

ADC

Timing:



A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16C73/74	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16LC73/74	2.0	—	—	µs	TOSC based, VREF full range
			PIC16C73/74	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16LC73/74	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5TAD	—	—	
132	TACQ	Acquisition time		Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

PIC16C74A

ADC

Specifiche elettriche:

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

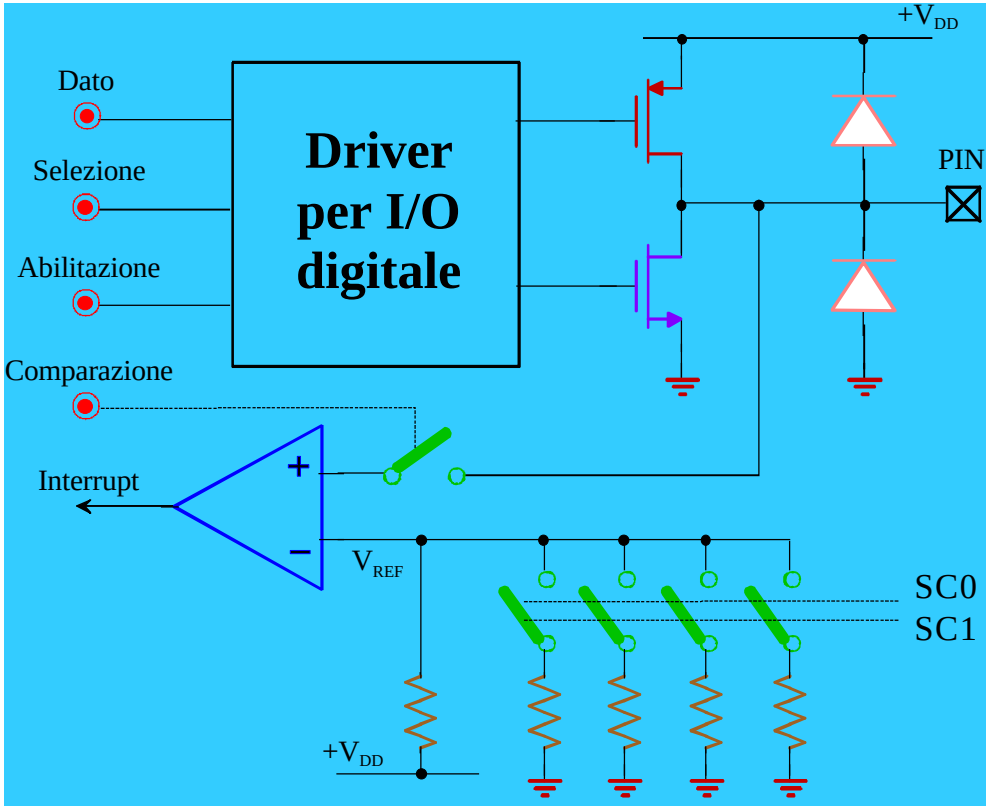
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

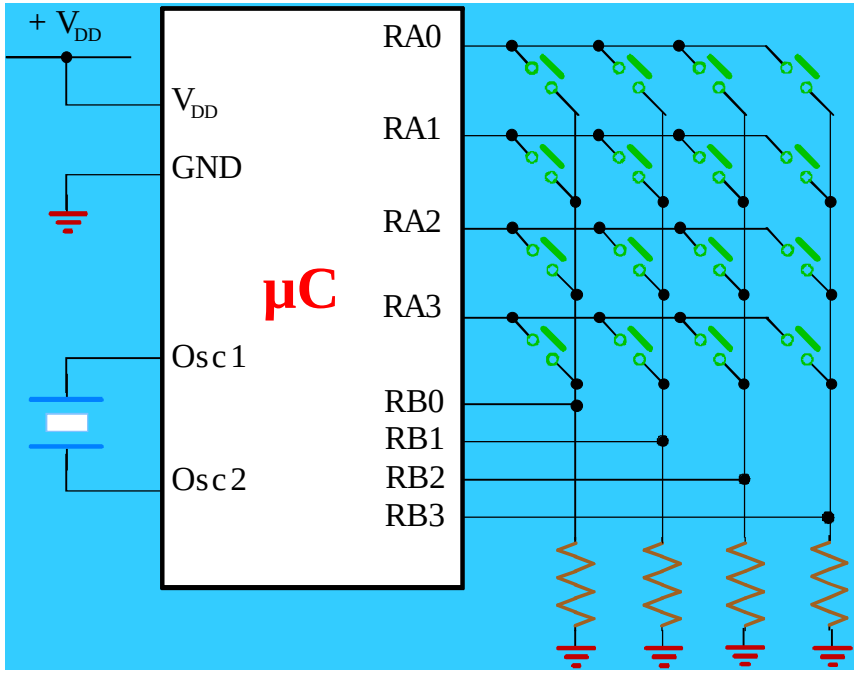
Comparatore o Watchdog analogico

Per monitorare un livello di tensione:



Esempi di impiego degli I/O

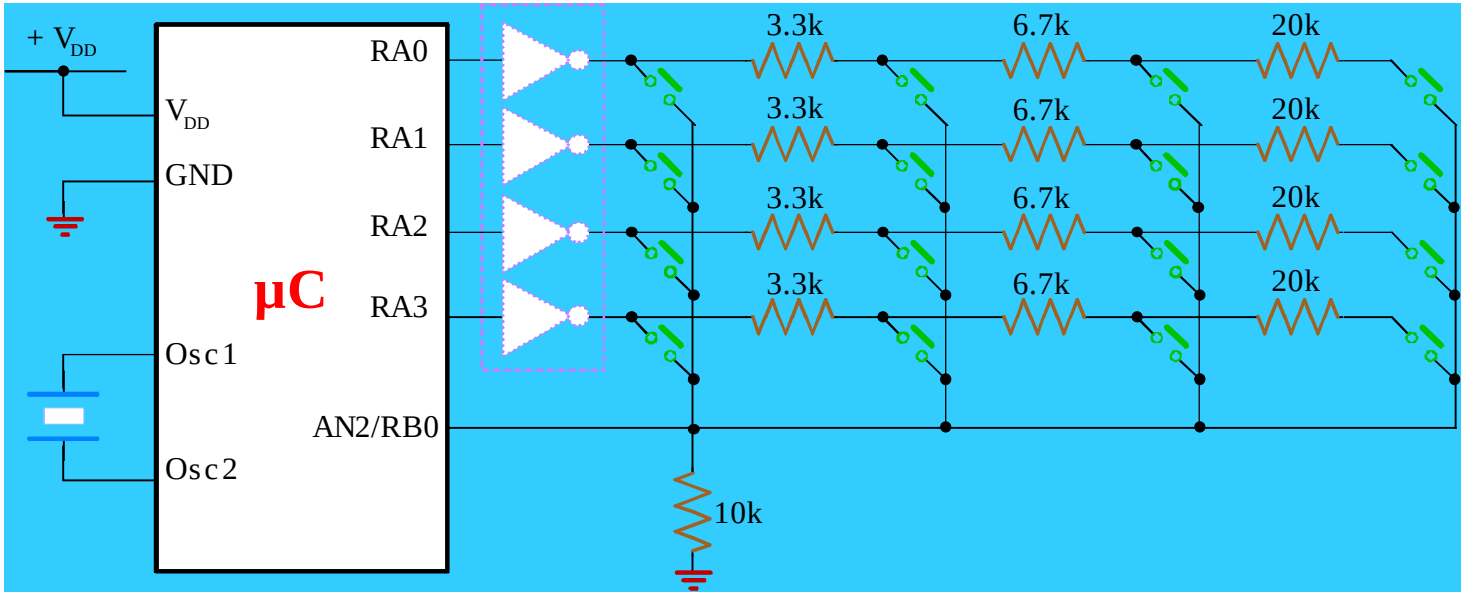
Esempio 1: Multiplexing Digitale di una tastiera



Si risparmiano linee digitali

Esempi di impiego degli I/O

Esempio 2: Acquisizione analogica



Colonna premuta	Tensione
1ª	5V
2ª	3.75V
3ª	2.5V
4ª	1.25V
nessuna	0V

Si utilizza un ritorno analogico
Gli si può fare scatenare un interrupt, ma...

$$V_{max,min} = 5 \cdot \frac{(10K \pm 10\%)}{(10K \pm 10\%) + (3.3K + 6.7K + 20K\ m10\%)}$$

$$V_{max,min} = 5 \cdot \frac{(10K \pm 10\%)}{(10K \pm 10\%) + (3.3K + 6.7K\ m10\%)}$$