Fondamenti di Elettronica - Ingegneria Elettronica -2008/09
Midterm Examination – November 21st, 2008

State clearly the question you are answering. E.g. 1a).
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

Exercise 0 –Mandatory (otherwise all the other exercises will not be corrected).

Consider the circuit shown in Fig. 1a.

Draw in a time diagram, providing values for all the relevant points, the curve of the voltage V_{out}(t) when the input current is the one shown in Fig. 1b.

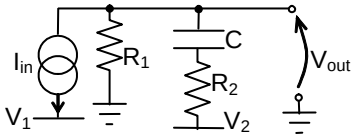

Fig. 1a

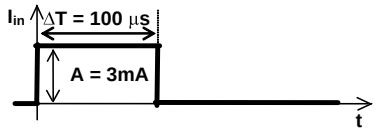

Fig. 1b

R_1=3kΩ R_2=6kΩ
C=220pF
V_1=-2V V_2=-1V

Exercise 1

Again referring to the circuit shown in Fig. 1a.

a) **Determine the charge stored in the capacitor *C* when the steady state is reached following the application of the signal shown in Fig. 1b. Provide justification for your answer.**

b) How the value of the stored charge in the capacitor *C* (already calculated in a) would change a long time after the application of the pulse shown in Fig. 1b if the pulse duration would be 1 μs. Provide justification for your answer.

Exercise 2

Let's refer to the *MOSFET* circuit shown in Fig. 2, in which *I* is a DC current generator.

a) Find the DC voltages at all nodes and the DC current in all branches.

b) **Find the small-signal voltage gain v_{out}/v_{in}. at low frequency (C open circuit).**

c) Find the value of the capacitor *C* that allows the circuit properly amplifying signals in the frequency band [100 Hz, 1.5 MHz].

d) How would change the DC bias voltages and currents computed in a) and the small signal gain computed in b) if the current generator *I* would be a non ideal current generator with an output resistance equal to *120 kΩ*.

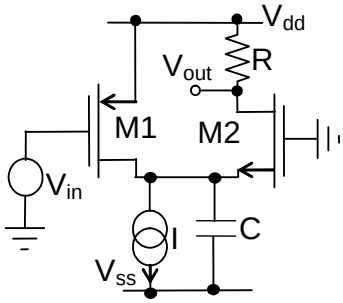

Fig. 2

$½\mu_p C_{ox}$=20 μA/V²
$(W/L)_p$=1
$½\mu_n C_{ox}$=50 μA/V²
$(W/L)_n$=2
$V_{Tn}=|V_{Tp}|$=0.5V
R=20kΩ
I=0.2mA
V_{dd}=+3V
V_{ss}=-3V

Exercise 3

Let's consider the CMOS logic gate shown in Fig. 3, that implements the logic function $Y = \overline{(A \cdot B \cdot C)} + \overline{A} + \overline{D}$.

a) Implement the following function in conventional CMOS, drawing the pull-up and the pull-down networks and justifying all the choices.

Let's suppose to short-circuit all the inputs together and let's consider the equivalent inverter.

b) Find the analog voltage range of the output node *Y* that ensures the operation of the equivalent *pMOSFET* in the saturation region.

c) Compute the time needed for the equivalent *pMOSFET* to exit from the saturation region after the transition of the input.

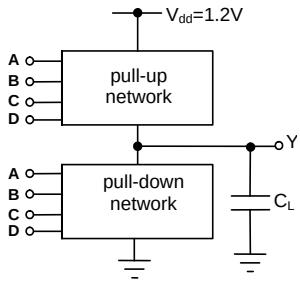

Fig. 3

$½\cdot\mu_n C_{ox}$ = 50 μA/V²
$½\cdot\mu_p C_{ox}$ = 20 μA/V²
$|V_{Tp}| = V_{Tn}$ = 0.45V
$(W/L)_n$ = 5
$(W/L)_p$ = 5
C_L = 1.6 pF

Exercise 4

Let us consider the circuit shown in Fig. 4. The diodes D_1 and D_2 are on when forward biased with *0.7* V. The current I_{in} is sinusoidal with frequency *f = 2 kHz* and amplitude *A = 1 mA*.

Draw in a time diagram, providing values for all the relevant points, the curve of the power dissipated by the diode D_2.

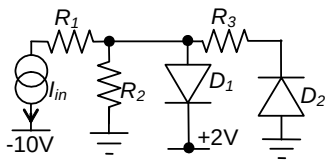

Fig. 4a

R_1=1 kΩ R_2=2kΩ R_3=3kΩ