Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2009/10
2nd Examination – September 13th, 2010

State clearly the question you are answering. E.g. 1a).
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

Exercise 1

Let us consider the circuit for the amplification and the conversion of signals shown in Fig. 1. The ADC is of the staircase type and features *n bits*.

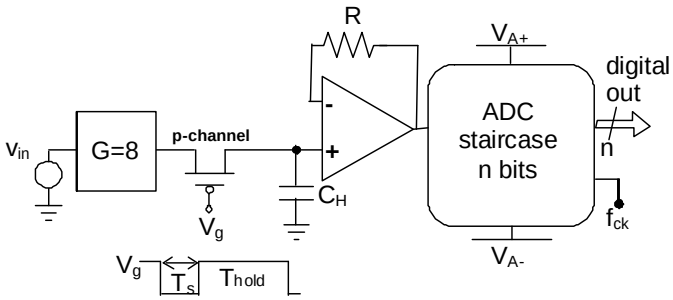

Fig. 1

$R = 10\ k\Omega$
$|V_{Tp}| = 0.8\ V$
$|k_p| = \frac{1}{2}\mu_p C_{ox}(W/L) = 20\ mA/V^2$
$V_{A+} = |V_{A-}| = 2.5\ V$
$f_{ck} = 30\ MHz$

a) Find the maximum number of bits that the ADC can feature in order to properly sample and convert a sinusoidal signal v_{in} with frequency $f = 15\ kHz$, assuming the minimum sample-time, equal to $1/f_{ck}$. Compute the best resolution that can be guaranteed at the input.

b) Find the voltage V_G to be applied to the gate of the MOSFET switch that guarantees a resistance virtually equal to infinity with *3 V* margin during the Hold phase and a resistance not higher than *25* Ω during the Sample phase, if the input signal is sinusoidal with amplitude equal to *300 mV*.

c) Under the hypothesis that the operational amplifier features a *Slew-Rate SR = 8 V/*μ*s* and the ADC features a number of *bits*, *n*, equal to *11*, find the maximum sampling frequency that ensures a conversion error lower than *1 LSB*, with signals of the maximum dynamics.

d) If the operational amplifier has a differential input resistance $R_{id} = 50\ M\Omega$ and a low frequency open-loop gain $A_0 = 80\ dB$, find the minimum value of the capacitor C_H that ensures a *droop rate* lower than *0.5 mV/ms*.

Exercise 2

Let us consider the circuit shown in Fig. 2 and assume that the operational amplifiers saturate at the bias voltages.

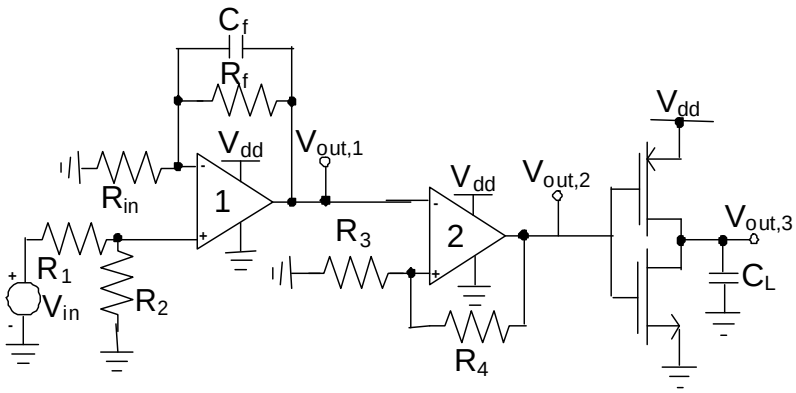

Fig. 2

$V_{dd} = 3.3\ V$
$R_{in} = 4\ k\Omega$
$R_f = 40\ k\Omega$
$C_f = 2\ pF$
$R_1 = 1\ k\Omega$
$R_2 = 2\ k\Omega$
$R_3 = 0.5\ k\Omega$
$R_4 = 5\ k\Omega$
$C_L = 4\ pF$
$V_{Tn} = |V_{Tp}| = 0.7\ V$
$\frac{1}{2}\mu_p C_{ox} = 30\ \mu A/V^2$
$(W/L)_p = 20$
$\frac{1}{2}\mu_n C_{ox} = 75\ \mu A/V^2$
$(W/L)_n = 8$

a) Draw the Bode magnitude plot of the transfer function $v_{out,1}/v_{in}$ assuming the operational amplifier ideal and providing values for all the relevant points.

b) Draw the transfer characteristic $v_{out,2}/v_{out,1}$, providing values for all the relevant points.

c) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $v_{out,3}(t)$, when the output signal of the second operational amplifier, $v_{out,2}$, is a square wave with frequency $f = 10MHz$, keeping into account the propagation times of the inverter.

d) If the first operational amplifier features an open-loop gain $A(s) = A_o/(1+s\tau_0)$, where $A_0 = 80\ dB$ and $\tau_0 = 15\ ms$, find the phase margin of the amplifier.

e) Find the minimum amplitude of the signal v_{in} that triggers the transition of the output $v_{out,3}$ and find the maximum current flowing from V_{dd} to ground through the transistors during the transition.