Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2012/13
Midterm Examination – May 10th, 2013

State clearly the question you are answering. E.g. 1a). Solve first questions in bold.
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

EXERCISE 0 –BOLD QUESTIONS MANDATORY (otherwise all the other exercises will not be corrected).

Consider the circuit shown in Fig. 1a.

Find the circuit time constant and the asymptotic values of the output voltage V_{out}, for t tending to $+\infty$ and to $-\infty$, when the input voltage is the signal shown in Fig. 1b.

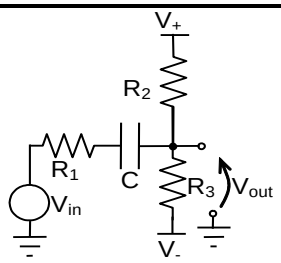

Fig. 1°

$R_1=3k\Omega$
$R_2=3k\Omega$
$R_3=1k\Omega$
$C=1nF$
$V_-=-1V$
$V_+=+3V$

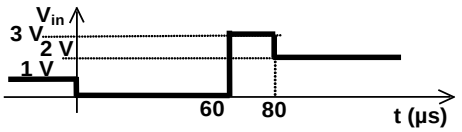

Fig. 1b

Exercise 1

Let's consider again the circuit shown in Fig. 1a.

a) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b *(non-periodic)*. Provide justification for your answer.

b) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1c *(non-periodic)*. Provide justification for your answer.

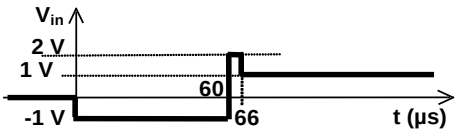

Fig. 1c

Exercise 2

Let's refer to the MOSFET circuit shown in Fig. 2. v_{in} is a small signal voltage generator.

a) Find the value of the form factor $(W/L)_2$ of transistor $M2$ that guarantees a bias current of *1 mA* flowing in $M2$. Find, then, the DC voltages at all the nodes and the DC current in all the branches

b) Find the small-signal voltage gain $v_{out,2}/v_{in}$ at low frequency (i.e. consider C as open circuit).

c) Find the singularities introduced by capacitors C in the transfer function v_{out}/v_{in}.

d) Find the maximum allowed value for resistor R_d that guarantees that both transistors are operating in saturation.

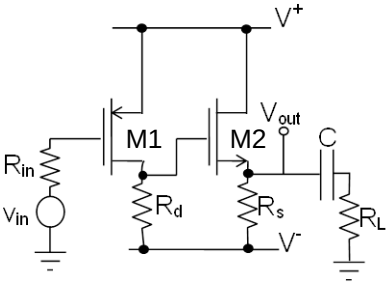

Fig.2

$\frac{1}{2}\mu_n C_{ox}=100\ \mu A/V^2$
$|k_p|=\frac{1}{2}\mu_p C_{ox}(W/L)_p=$
$=100\ \mu A/V^2$
$V_{Tn} = |V_{Tp}| = 1V$
$R_{in}=50\Omega$
$R_s=900\Omega$
$C=47nF$
$R_d=3k\Omega$
$R_L=10k\Omega$
$V^+=+5V$
$V^-=-5V$
$r_0 = \infty$.

Esercizio 3

Let's consider the CMOS logic gate shown in Fig. 3, that implements the logic function $Y=\overline{[A\cdot(B+C)]\cdot A\cdot D}$.

a) Implement the logic function in conventional CMOS technology in its minimal form, drawing the pull-up and the pull-down networks and justifying all the choices.

b) Determine the transistion featuring the shortest transition time and compute such transistion time.

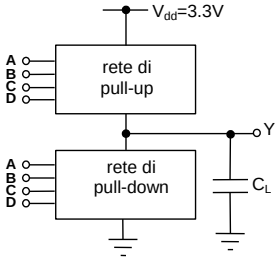

Fig. 3

$k_n=\frac{1}{2}\cdot\mu_n C_{ox}(W/L)_n = 100\ \mu A/V^2$
$|k_p|=\frac{1}{2}\cdot\mu_p C_{ox}(W/L)_p = 40\ \mu A/V^2$
$|V_{Tp}| = V_{Tn} = 0.7V$
$C_L = 20\ pF$

Exercise 4

Let us consider the circuit shown in Fig. 4. The diodes D_1 and D_2 are on when forward biased with *0.7 V*. The voltage V_{in} varies in the range *[-10V, +10V]*.

a) Draw the input-output transfer curve ($V_{out}(t)$ vs. $V_{in}(t)$), providing justification for your answer.

b) Find the minimum value of the break-down voltage that diode D_2 should feature to avoid its operation in the break-down region.

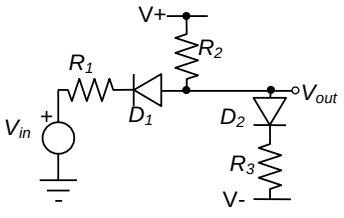

Fig. 4

$V^+=10V$
$V^-=-10V$
$R_1=20\ k\Omega$
$R_2=10\ k\Omega$
$R_3=20\ k\Omega$