Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2012/13
Unscheduled Examination – May 10th, 2013

State clearly the question you are answering. E.g. 1a). Solve first questions in bold.
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

Exercise 1

Let's consider the circuit shown in Fig. 1a.

a) **Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b *(non-periodic)*. Provide justification for your answer.**

b) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1c *(non-periodic)*. Provide justification for your answer.

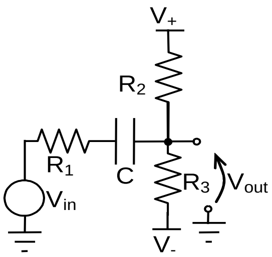


Fig. 1a

$R_1=3k\Omega$
$R_2=3k\Omega$
$R_3=1k\Omega$
$C=1nF$
$V_-=-2V$
$V_+=+2V$

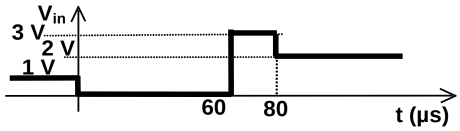


Fig. 1b

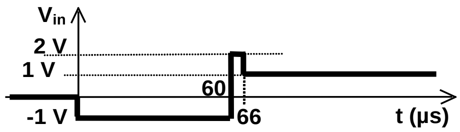


Fig. 1c

Exercise 2

Let's refer to the MOSFET circuit shown in Fig. 2. v_{in} is a small signal voltage generator.

a) **Find the value of the form factor $(W/L)_2$ of transistor *M2* that guarantees a bias current of *1 mA* flowing in *M2*. Find, then, the DC voltages at all the nodes and the DC current in all the branches**

b) **Find the small-signal voltage gain $v_{out,2}/v_{in}$ at low frequency (i.e. consider *C* as open circuit).**

c) Draw the magnitude Bode diagram of the small signal voltage transfer v_{out}/v_{in}.

d) Find the maximum allowed value for resistor R_d that guarantees that both transistors are operating in saturation.

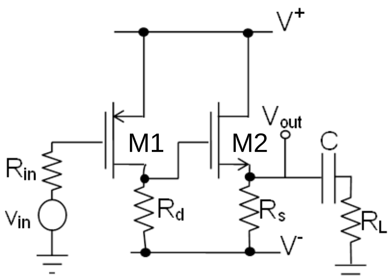
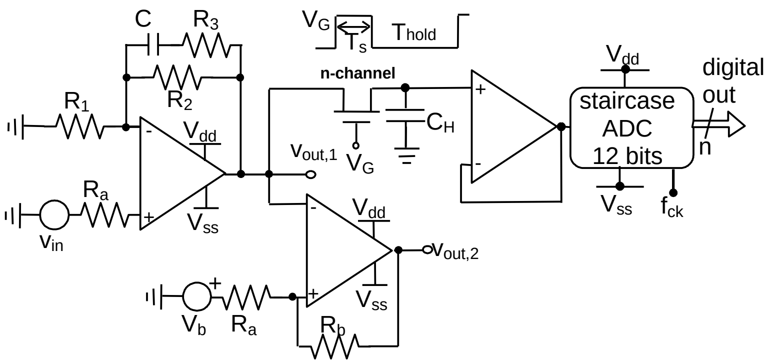


Fig.2

$½\mu_nC_{ox}=100\ \mu A/V^2$
$|k_p|=½\mu_pC_{ox}(W/L)_p==100\ \mu A/V^2$
$V_{Tn}=|V_{Tp}|=1V$
$R_{in}=50\Omega$
$R_s=900\Omega$
$C=47nF$
$R_d=3k\Omega$
$R_L=10k\Omega$
$V^+=+5V$
$V^-=-5V$
$r_0=\infty.$

Exercise 3

Let us consider the data acquisition system shown in Fig. 3. Let us assume that the operational amplifier saturates at the power supply voltages.



$C=47pF$
$R_1=1k\Omega$
$R_2=19k\Omega$
$R_3=10k\Omega$
$R_a=2k\Omega$
$R_b=3k\Omega$
$V_{dd}=+5V$
$V_{ss}=-5V$
$k_n=½\mu_nC_{ox}(W/L)_n=5\ mA/V^2$
$V_{Tn}=1V$

Fig. 3

a) **Draw the diagram of the input-output transfer characteristics ($v_{out,2}/v_{out,1}$), quoting all the relevant points and showing the reasoning performed to compute the behaviour of the transfer characteristics.**

b) **Draw the magnitude Bode diagram of the transfer function $V_{out,1}/V_{in}$, quoting all the relevant points.**

c) **Let's consider a DC input voltage equal to *-100mV*. Find the limiting values of the drive voltage to be applied to the gate of the MOS transistor able to guarantee an ideally infinite resistance $R_{ds,off}$ during the Hold phase and a resistance $R_{ds,on}$ below 8 Ω in the Sample phase.**

d) Determine the minimum value of the Hold capacitor (C_H) that guarantees that a droop rate below ½ *LSB/ms*, if the opamp used for the buffer features a differential input resistance $R_{id}=10\ M\Omega$ and an open loop gain $A_0=70dB$.

e) Find the minimum value of the ADC clock frequency needed to properly sample a *10 kHz* input sinusoidal signal, if the ADC is based on the staircase working principle (Let's assume a duration of the Sample Phase equal to the clock period).