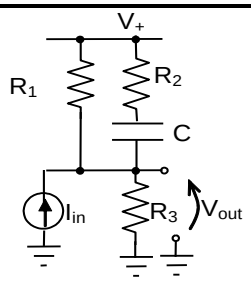
Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2013/14
Midterm Examination – May 9th, 2014

State clearly the question you are answering. E.g. 1a). Solve first questions in bold.
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

EXERCISE 0 –BOLD QUESTIONS MANDATORY (otherwise all the other exercises will not be corrected).

Consider the circuit shown in Fig. 1a.

Find the circuit time constant and the asymptotic values of the output voltage V_{out}, for t tending to $+\infty$ and to $-\infty$, when the input voltage is the signal shown in Fig. 1b (*non-periodic*), if $T = 50$ µs.



$R_1=10k\Omega$
$R_2=5k\Omega$
$R_3=20k\Omega$
$C=300pF$
$V_+=+6V$

Fig. 1a

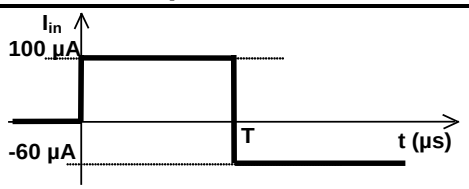


Fig. 1b

Exercise 1

Let's consider again the circuit shown in Fig. 1a.

a) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b *(non-periodic)*, if $T = 50$ µs. Provide justification for your answer.

b) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b *(non-periodic)*, if $T = 3.5$ µs. Provide justification for your answer.

Exercise 2

Let's refer to the MOSFET circuit shown in Fig. 2. v_{in} is a small signal voltage generator.

a) Find the circuit bias point (i.e. the DC voltages at all the nodes and the DC current in all the branches).

b) Find the small-signal voltage gain v_{out}/v_{in} at low frequency (i.e. consider C_1 e C_{out} as open circuit).

c) Find the singularities introduced by capacitors C_1 e C_{out} in the transfer function v_{out}/v_{in}.

d) Find the maximum allowed range for the output voltage that guarantees that both transistors are operating in saturation.

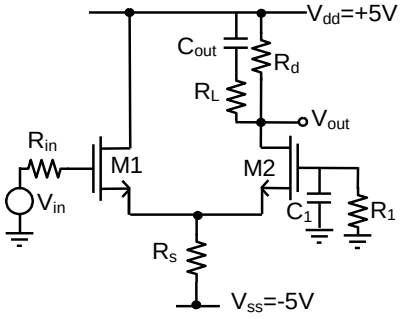


Fig.2

$k_n=½\mu_nC_{ox}(W/L)_n=$
$=1\ mA/V^2$
$V_{Tn} = 0.7\ V$
$R_{in} =500\ \Omega$
$R_1 =500\ k\Omega$
$R_s = 1.65\ k\Omega$
$C_1=470nF$
$C_{out}=10nF$
$R_d = 4.5\ k\Omega$
$R_L = 4.5\ k\Omega$
$r_0 = \infty.$

Exercise 3

Let's consider the CMOS logic gate shown in Fig. 3, that implements the logic function $Y = \overline{(A+B)\cdot(C+A)}$.

a) Implement the logic function in conventional CMOS technology in its minimal form, drawing the pull-up and the pull-down networks and justifying all the choices.

b) Find the minimum time needed for the output to switch from V_{dd} to $(V_{dd} - V_T)$, following an appropriate input transition.

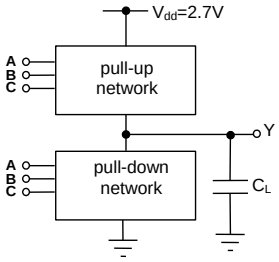


Fig. 3

$k_n=½\cdot\mu_n C_{ox}(W/L)_n = 100\ \mu A/V^2$
$|k_p|=½\cdot\mu_p C_{ox}(W/L)_p = 40\ \mu A/V^2$
$|V_{Tp}| = V_{Tn} = 0.7V$
$C_L = 12\ pF$

Exercise 4

Let us consider the circuit shown in Fig. 4a. The diodes D_1 and D_2 are on when forward biased with $0.7\ V$. Fig. 4b shows the time diagram of the input voltage V_{in}.

Draw the time diagram of the output voltage $V_{out}(t)$, quoting all the relevant points and providing adequate justification for your answer.

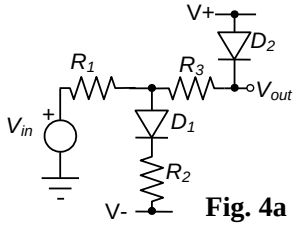


Fig. 4a

$V^+=2V$ $V^-=-2V$
$R_1=2\ k\Omega$ $R_2=10\ k\Omega$ $R_3=4\ k\Omega$

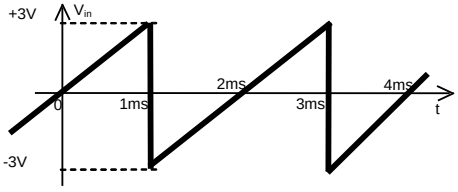


Fig. 4b