Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2014/15
Midterm Examination – May 7th, 2015

State clearly the question you are answering. E.g. 1a). Solve first questions in bold.
Solve first questions in bold. This is a 3-hour in-class closed-book exam

EXERCISE 0 – MANDATORY
(otherwise all the other exercises will not be corrected).

Consider the circuit shown in Fig. 1a.
Find the circuit time constant and the average value of the output current I_{out}, when the input voltage is the signal shown in Fig. 1b (*periodic*), if $T = 48$ *ms*.

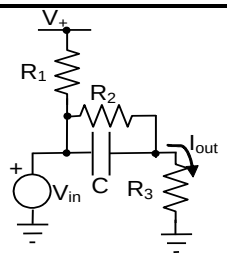

Fig. 1a

$R_1=1k\Omega$
$R_2=3k\Omega$
$R_3=4k\Omega$
$C=200nF$
$V_+=+3V$

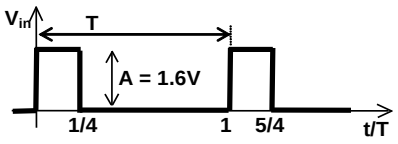

Fig. 1b

Exercise 1

Let's consider again the circuit shown in Fig. 1a.

a) Draw in a time diagram, providing values for all the relevant points, the curve of the current $I_{out}(t)$, when the input voltage is the one shown in Fig. 1b *(periodic)*, if $T = 48$ *ms*. Provide justification for your answer.
b) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $I_{out}(t)$, when the input voltage is the one shown in Fig. 1b *(periodic)*, if $T = 2.4$ *ms*. Provide justification for your answer.

Exercise 2

Let's refer to the MOSFET circuit shown in Fig. 2. i_{in} is a small signal current generator.

a) Find the value of resistor R_s that provides *1 mA* static current in the transistor. Find, then, the circuit bias point (i.e. the DC voltages at all the nodes and the DC current in all the branches).
b) Find the small-signal transfer function v_{out}/i_{in} at high frequency (C e C_2 short-circuited).
c) Find the singularities introduced by capacitors C e C_2 in the transfer function v_{out}/i_{in}.
d) Find the maximum current amplitude, in the case of a sinusoidal signal at *5 Hz* frequency, that ensures a linearity error below or equal to 4%.

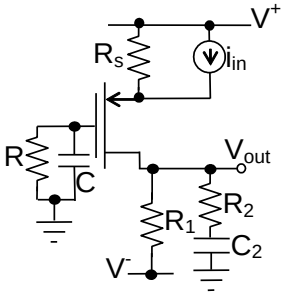

Fig. 2

$V+ = -V^- = 4\ V$
$|k_p| = \frac{1}{2}\mu_p C_{ox}(W/L)_p = 1\ mA/V^2$
$V_{Tp} = -1\ V$
$R = 2.5\ M\Omega$
$R_1 = 4\ k\Omega$
$C = 220nF$
$C_2 = 47nF$
$R_2 = 4\ k\Omega$
$r_0 = \infty$.

Exercise 3

Let's consider the CMOS logic gate shown in Fig. 3, that implements the logic function $Y = \overline{(A+B)\cdot(C+D)} + \overline{A}\cdot\overline{B}$.

a) Implement the logic function in conventional CMOS technology in its minimal form, drawing the pull-up and the pull-down networks and justifying all the choices.
b) Find the maximum time interval, following an low-high output switch, during which the trasistors that switch on are biased in the saturation region.

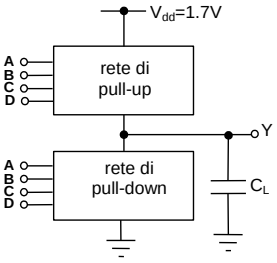

Fig. 3

$k_n = \frac{1}{2}\cdot\mu_n C_{ox}(W/L)_n = 200\ \mu A/V^2$
$|k_p| = \frac{1}{2}\cdot\mu_p C_{ox}(W/L)_p = 60\ \mu A/V^2$
$|V_{Tp}| = V_{Tn} = 0.65V$
$C_L = 650\ fF$

Exercise 4

Let us consider the circuit shown in Fig. 4a. The diode is on when forward biased with *0.7 V* and operates in the breakdown region if the reverse voltage overcomes *4.7 V*.

Draw the transfer characteristics V_{out} *vs.* V_{in}, quoting all the relevant points and providing adequate justification for your answer, assuming that the input current varies in the interval [*-2 mA*; *2 mA*].

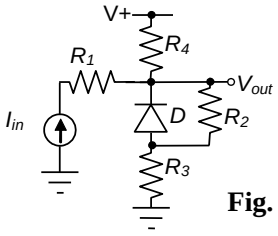

Fig. 4a

$V^+ = 3V$
$R_1 = 1\ k\Omega$
$R_2 = 3\ k\Omega$
$R_3 = 2\ k\Omega$
$R_4 = 4\ k\Omega$