Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2009/10
Midterm Examination – May 6th, 2010

State clearly the question you are answering. E.g. 1a).
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

EXERCISE 0 –MANDATORY (otherwise all the other exercises will not be corrected).

Consider the circuit shown in Fig. 1a.

a) **Find the average value of the current I_{out} when the input current is the one shown in Fig. 1b.**
b) **Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b. Provide justification for your answer.**

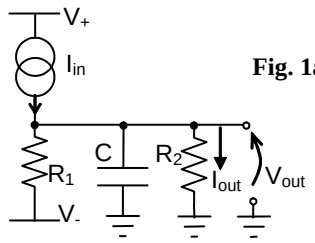

Fig. 1a

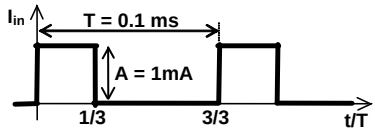

Fig. 1b

$R_1=3k\Omega$ $R_2=1k\Omega$ $C=100pF$ $V_+=+5V$ $V_-=-4V$

Exercise 1

Let's refer to the *MOSFET* circuit shown in Fig. 2.

a) Find the DC voltages at all nodes and the DC current in all branches.
b) Find the small-signal voltage gain v_{out}/v_{in} at low frequency (C open circuit).
c) Find the singularities introduced by the capacitor C in the transfer function v_{out}/v_{in}.
d) Determine the maximum value of the resistor R_1 that allows "proper operation" of the circuit, considering the behavior at low frequency (C open circuit).

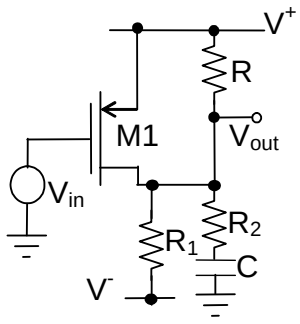

Fig. 2

$\frac{1}{2}\mu_p C_{ox}=25\ \mu A/V^2$
$(W/L)_p=10$
$|V_{Tp}|=1V$
$R=1M\Omega$
$R_1=1k\Omega$
$R_2=2k\Omega$
$C=200pF$
$V^+=+5V$
$V^-=-5V$

Exercise 2

Let's consider the CMOS logic gate shown in Fig. 3, that implements the logic function $Y = \overline{A \cdot (B + C + A)} \cdot D \cdot \overline{E}$.

a) Implement the logic function in conventional CMOS technology in its minimal form, drawing the pull-up and the pull-down networks and justifying all the choices.
b) Find the combination of the inputs that determines the fastest *LH* and *HL* transitions and compute those transition times.
c) Compute the power dissipated by the logic gate if inputs *B* and C are both driven by a clock signal with *1 MHz* frequency, input *A* is kept high and inputs *D* and *E* are kept low.

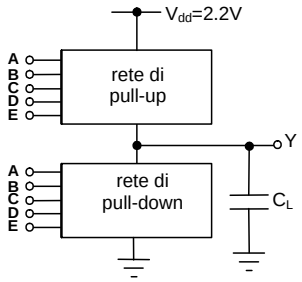

Fig. 3

$\frac{1}{2}\cdot\mu_n C_{ox} = 100\ \mu A/V^2$
$\frac{1}{2}\cdot\mu_p C_{ox} = 40\ \mu A/V^2$
$|V_{Tp}| = V_{Tn} = 0.65V$
$(W/L)_n = 3$
$(W/L)_p = 5$
$C_L = 2.1\ pF$

Exercise 3

Let us consider the circuit shown in Fig. 4. The diode *D* is on when forward biased with *0.7 V*. The voltage V_{in} is a sinusoidal signal with frequency $f = 5\ kHz$ and amplitude $A = 5\ V$.

a) Draw in a time diagram, providing values for all the relevant points, the curve of the current $I_{out}(t)$.
b) If the diode features a break-down voltage $|V_{BD}|=5V$, draw in a time diagram, providing values for all the relevant points, the curve of the power dissipated by the diode.

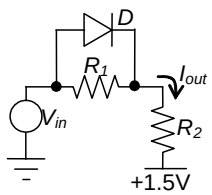

Fig. 4

$R_1=1\ k\Omega$ $R_2=2k\Omega$