Fondamenti di Elettronica - Ingegneria Elettronica -2008/09
First Examination – March 5th 2009

State clearly the question you are answering. E.g. 1a).
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

Exercise 1

Consider the amplifying circuit shown in Fig. 1.

a) Find the value of the resistor R_0 that provides a 0.5mA bias current in each transistor of the differential pair and, then, find the full circuit biasing.

b) Find the expression and the value of the small signal differential gain $(v_{out,2}-v_{out,1})/(v_2-v_1)$.

c) Find the expression and the value of the small-signal common-mode gain $(v_{out,2}+v_{out,1})/(v_2+v_1)$.

d) If the gate of transistor M_2 is at a fixed voltage in small-signal conditions (i.e. $v_2=0V$ in small-signal conditions), find the expression and the value of the small-signal gain $(v_{out,2}- v_{out,1})/v_1$.

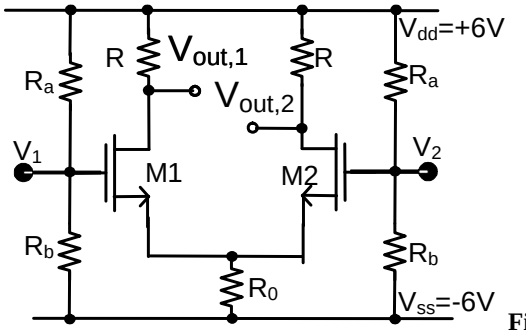

Fig. 1

$k_n=\frac{1}{2}\mu_n C_{ox}(W/L)=0.5mA/V^2$ $V_{Tn}=0.5V$
$R_a=70k\Omega$ $R_b=50k\Omega$ $R=12k\Omega$

Exercise 2

Consider the 3-bit Digital-to-Analog Converter shown in Fig. 2.

a) Let's assume that the operational amplifier is ideal. Find the maximum current that can flow in the resistor R_f and the current that flows in R_f when the input digital word is 001.

b) Under the hypothesis that the operational amplifier has an offset voltage of *8mV*, find the input digital word that causes the maximum contribution of the offset voltage to the output and compute the expression and the value of such contribution.

c) If the gain-bandwidth product of the operational amplifier is *GBWP = 10MHz*, draw the time evolution of the output voltage when the input digital word changes from *100* to *111*, quoting all the significant points.

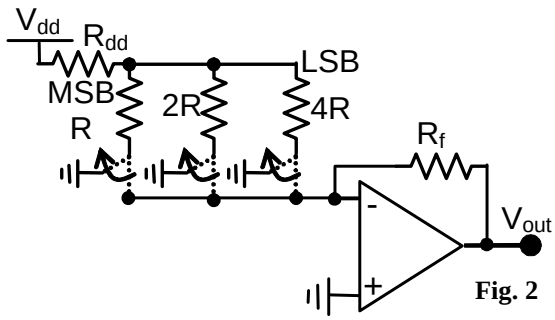

Fig. 2

$V_{dd}=5V$ $R_{dd}=200\Omega$ $R=2k\Omega$ $R_f=1k\Omega$

Exercise 3

Consider the logic circuit shown in Fig. 3, in which the logic signals A, B, C, D are either 0V (logic '0') or +5V (logic '1'). Assume that the on-voltage of the diode is 0V.

a) Find the logic function implemented by the circuit, writing the truth table and justifying your answer.

b) Implement the logic function found in a) in CMOS logic justifying all the choices.

c) In the case of the logic circuit determined in b), let's suppose to short-circuit the inputs *A* and *B* and to drive them with an $f_1 = 100\ kHz$ square-wave and the inputs *C* and *D* and to drive them with an $f_2 = 1\ MHz$ square-wave. Find the dynamic power dissipation justifying the answer, if the circuit drives an output capacitive load equal to $C = 3pF$.

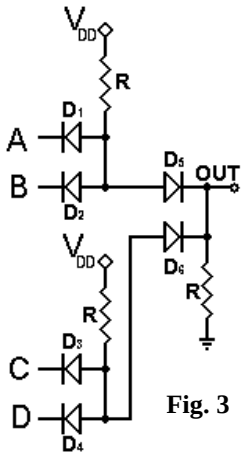

Fig. 3

$V_{DD}=5V$
$V_{Tn}=|V_{Tp}|=0.8V$
$k_n=200\mu A/V^2$
$k_p=80\mu A/V^2$