Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2011/12
Midterm Examination – May 3th, 2012

State clearly the question you are answering. E.g. 1a).
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

EXERCISE 0 –BOLD QUESTIONS MANDATORY (otherwise all the other exercises will not be corrected).

Consider the circuit shown in Fig. 1a.

a) **Find the average value of the voltage V_{out} when the input voltage is a sinusoidal signal with amplitude equal to *1 V* and frequency *1 kHz*.**

b) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b *(non-periodic)*. Provide justification for your answer.

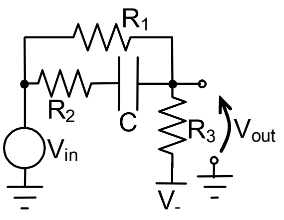
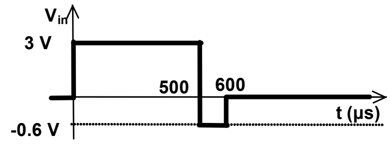


Fig. 1a



$R_1=10k\Omega$ $R_2=2.5k\Omega$ $R_3=2k\Omega$ $C=300pF$ $V_-=-2V$

Fig. 1b

Exercise 1

Let's refer to the MOSFET circuit shown in Fig. 2. v_{in} is a small signal voltage generator.

a) **Find the value of resistor R_s that guarantees a bias current of *1 mA* flowing in the MOSFET. Find, then, the DC voltages at all nodes and the DC current in all branches**

b) **Find the small-signal voltage gain $v_{out,2}/v_{in}$ at high frequency (i.e. consider all capacitances as short circuits).**

c) Find the small-signal voltage gain $v_{out,1}/v_{in}$ at low frequency (i.e. consider all capacitances as open circuits), assuming that the transistor features an output resistance $r_0 = 100k\Omega$.

d) Find the singularities introduced by the capacitors C_1 and C_2 in the transfer function $v_{out,1}/v_{in}$, assuming that the transistor features an output resistance $r_0 = \infty$.

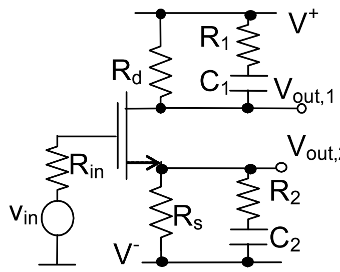


Fig. 2

$½\mu_nC_{ox}=50\ \mu A/V^2$ $(W/L)_n=5$ $V_{Tn}=0.8V$ $R_{in}=5k\Omega$ $R_2=500\Omega$ $C_2=700pF$ $R_d=5k\Omega$ $R_1=10k\Omega$ $C_1=50pF$ $V^+=+6V$ $V^-=-6V$

Exercise 2

Let's consider the CMOS logic gate shown in Fig. 3, that implements the logic function $Y=\overline{(A+B)\cdot(C+D\cdot E)\cdot A}$.

a) **Implement the logic function in conventional CMOS technology in its minimal form, drawing the pull-up and the pull-down networks and justifying all the choices.**

b) Compute the propagation delay of the gate, when all the inputs are short circuited and driven by a single logic signal.

c) Compute if the logic gate obtained when all the inputs are short circuited and driven by a 50% *duty-cycle*, *200MHz* frequency logic signal can properly switch. Justify your answer.

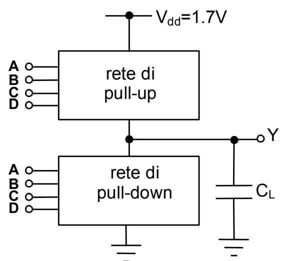


Fig. 3

$k_n=½\cdot\mu_n C_{ox}(W/L)_n = 100\ \mu A/V^2$
$|k_p|=½\cdot\mu_p C_{ox}(W/L)_p = 200\ \mu A/V^2$
$|V_{Tp}| = V_{Tn} = 0.5V$ $C_L=3\ pF$

Exercise 3

Let us consider the circuit shown in Fig. 4. The diodes D_1 and D_2 are on when forward biased with $0.7\ V$. The voltage V_{in} is a saw-tooth signal with period $T= 10\ ms$, peak-to-peak amplitude equal to $8\ V$ and zero mean value.

a) **Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$.**

b) If diode D_1 features a break-down voltage $V_{BD}=-5V$, draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$.

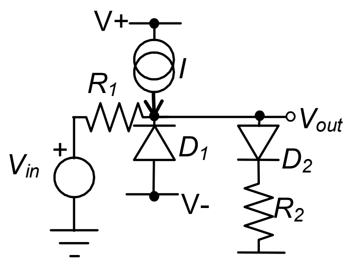


Fig. 4

$V^+=4V$
$V^-=-2V$
$I=100\mu A$
$R_1=1\ k\Omega$
$R_2=2\ k\Omega$