Fondamenti di Elettronica - Ingegneria Elettronica – a.a. 2011/12
Unscheduled Examination – May 3th, 2012

State clearly the question you are answering. E.g. 1a).
Solve first questions in bold. This is a 3-hour in-class closed-book exam.

Exercise 1

Consider the circuit shown in Fig. 1a.

a) Find the average value of the voltage V_{out} when the input voltage is a sinusoidal signal with amplitude equal to *1 V* and frequency *1 kHz*.

b) Draw in a time diagram, providing values for all the relevant points, the curve of the voltage $V_{out}(t)$, when the input current is the one shown in Fig. 1b *(non-periodic)*. Provide justification for your answer.

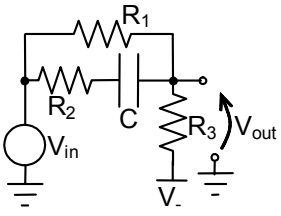
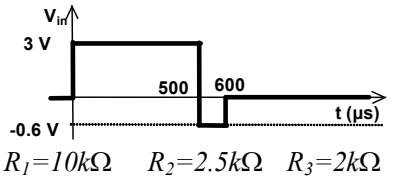


Fig. 1a



$R_1=10k\Omega$ $R_2=2.5k\Omega$ $R_3=2k\Omega$
$C=300pF$ $V_-=-2V$

Fig. 1b

Exercise 2

Let's refer to the MOSFET circuit shown in Fig. 2. v_{in} is a small signal voltage generator.

a) Find the value of resistor R_s that guarantees a bias current of *1 mA* flowing in the MOSFET. Find, then, the DC voltages at all nodes and the DC current in all branches

b) Find the small-signal voltage gain $v_{out,2}/v_{in}$ at high frequency (i.e. consider all capacitances as short circuits).

c) Find the small-signal voltage gain $v_{out,1}/v_{in}$ at low frequency (i.e. consider all capacitances as open circuits), assuming that the transistor features an output resistance $r_0 = 100k\Omega$.

d) Find the singularities introduced by capacitors C_1 and C_2 in the transfer function $v_{out,1}/v_{in}$, assuming that the transistor features an output resistance $r_0 = \infty$.

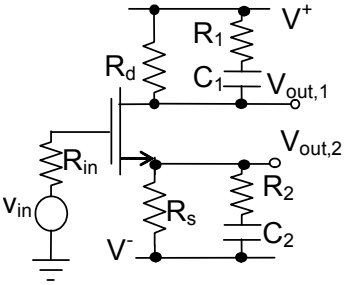


Fig. 2

$\frac{1}{2}\mu_n C_{ox}=50\ \mu A/V^2$ $(W/L)_n=5$ $V_{Tn}=0.8V$
$R_{in}=5k\Omega$ $R_2=500\Omega$ $C_2=700pF$
$R_d=5k\Omega$ $R_1=10k\Omega$ $C_1=50pF$
$V^+=+6V$ $V^-=-6V$

Exercise 3

Let us consider the circuit shown in Fig. 3. Let us assume that the operational amplifier saturates at the power supply voltages.

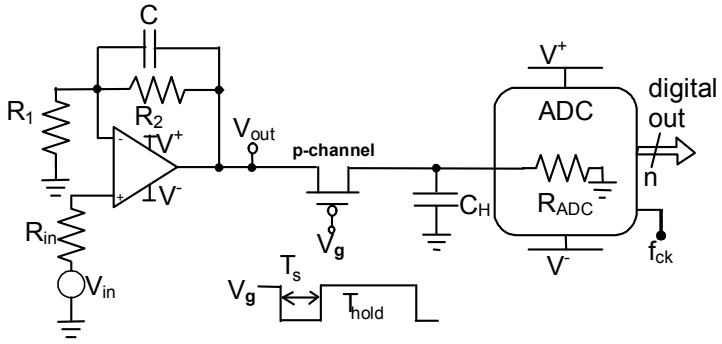


Fig. 3

$V^+=5V$
$V^-=-5V$
$R_1=1\ k\Omega$
$R_2=9\ k\Omega$
$R_{in}=50\ \Omega$
$C=20\ pF$
$|Vt_p|=0.8V$
$|k_p|=\frac{1}{2}\mu_p C_{ox}(W/L)=10mA/V^2$

a) Determine the expression of the ideal transfer function v_{out}/v_{in} and draw its magnitude Bode diagram, providing values for all the relevant points.

b) In presence of a signal at the amplifier output that covers the maximum dynamics, find the limiting values of the drive voltage to be applied to the gate of the MOS transistor able to guarantee a an ideally infinite resistance $R_{ds,off}$ during the Hold phase and a resistance $R_{ds,on}$ below 10 Ω in the Sample phase.

c) In presence of a DC input signal v_{in}, find the minimum voltage that can be distinguished from zero, if the *ADC* features *n = 10* bits.

d) If the operational amplifier gain-bandwidth product is *GBWP = 200 MHz* and its DC open loop gain is $A_0 = 75\ dB$, find the phase margin of the amplifying stage.

e) Determine the minimum value of the Hold capacitor (C_H) that guarantees that the *droop* is below ½ *LSB*, if the ADC is based on a successive approximation logic, features 10 *bits*, an input resistance (R_{ADC}) equal to *5 M*Ω and is driven with a clock frequency $f_{ck} = 10\ MHz$.